

AM64x/AM243x EVM BOARD

PROC101D

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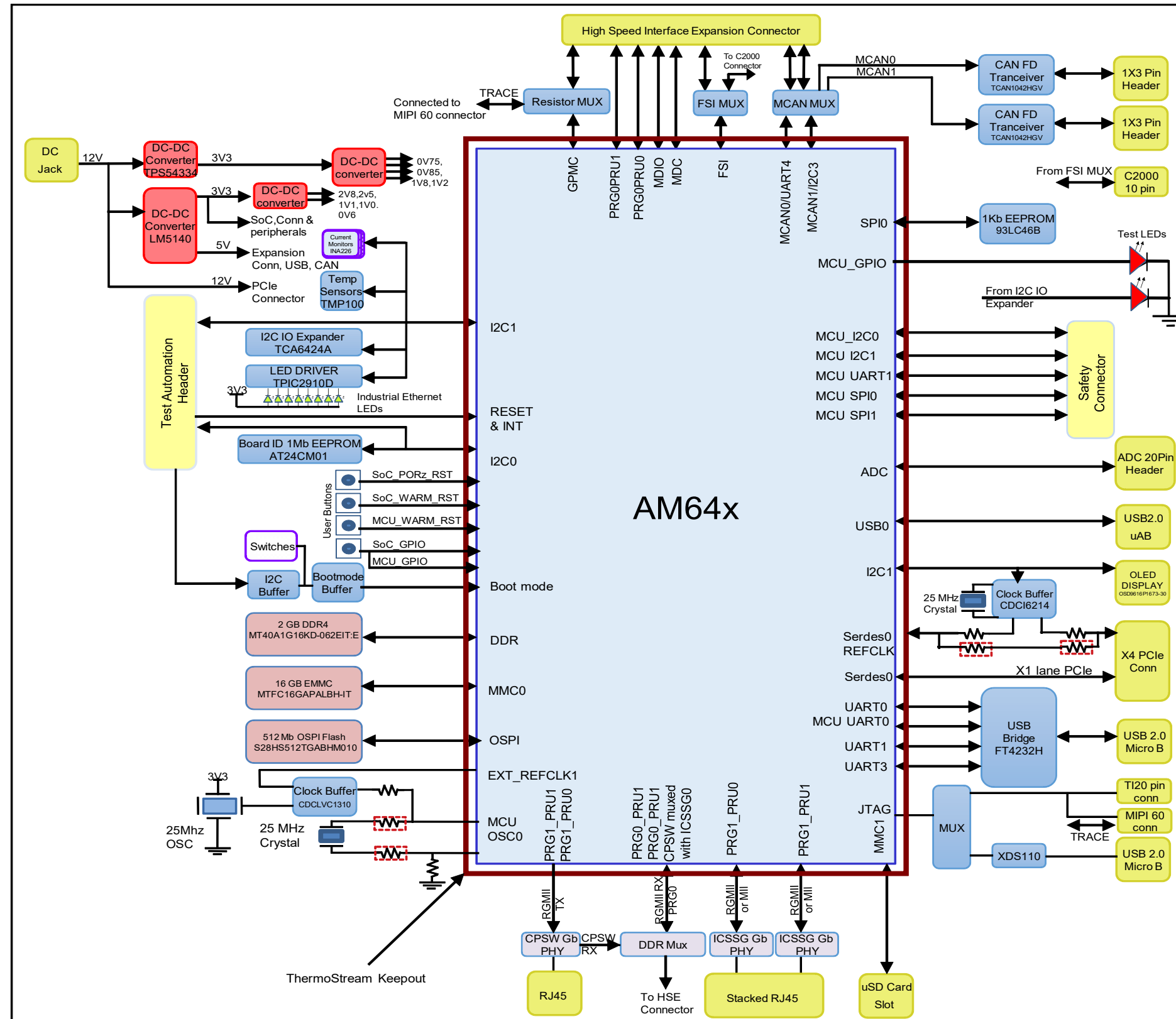
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REV	D
VER	1.2

REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	11th MARCH 2022	Drafted from "PROC101B_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	11th MARCH 2022	Removed Voltage Monitor circuit & added RC Delay Circuit for power down sequence requirement Fixed Power down sequence issue seen on AM243x REV B	Mistral Design Team	AJIT MB	AJIT MB
0.3	11th MARCH 2022	Updated schematics to support PG2 Silicon	Mistral Design Team	AJIT MB	AJIT MB
1.0	30th MARCH 2022	Baselined and Released	Mistral Design Team	AJIT MB	AJIT MB
1.1	5th AUG 2022	Updated SoC Part Number and OPN Details Updated SoC Symbol for Reserved pins	Mistral Design Team	AJIT MB	AJIT MB
1.2	27 NOV 2023	Reduced the switching frequency of U30 to 440 Khz for compliance testing (R.E) Resized the Inductors (L5 & L6), Capacitors (C69, C71, C81 & C82) for the change in SW frequency of U30	Mistral Design Team	AJIT MB	AJIT MB

BLOCK DIAGRAM_AM64x_EVM



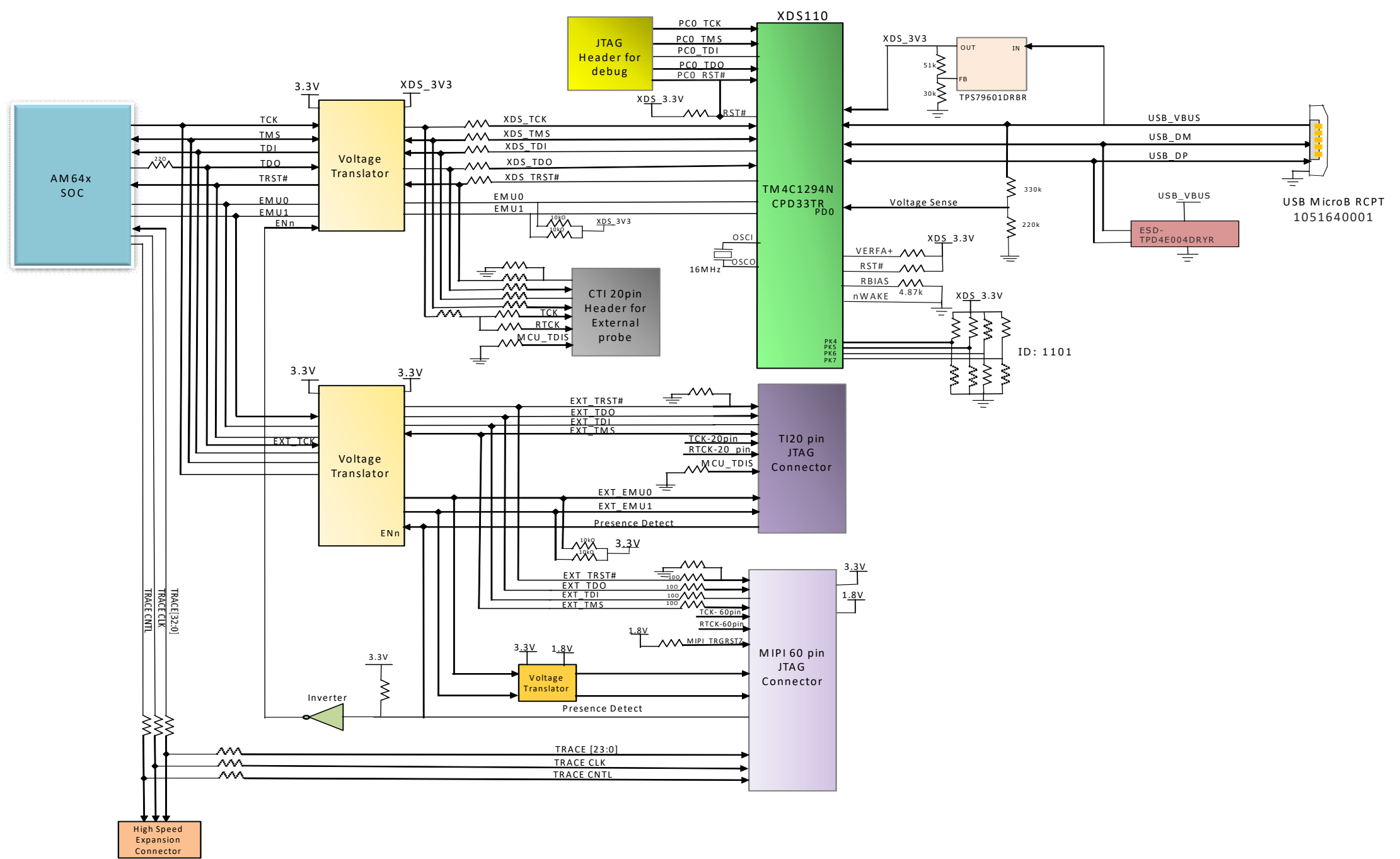
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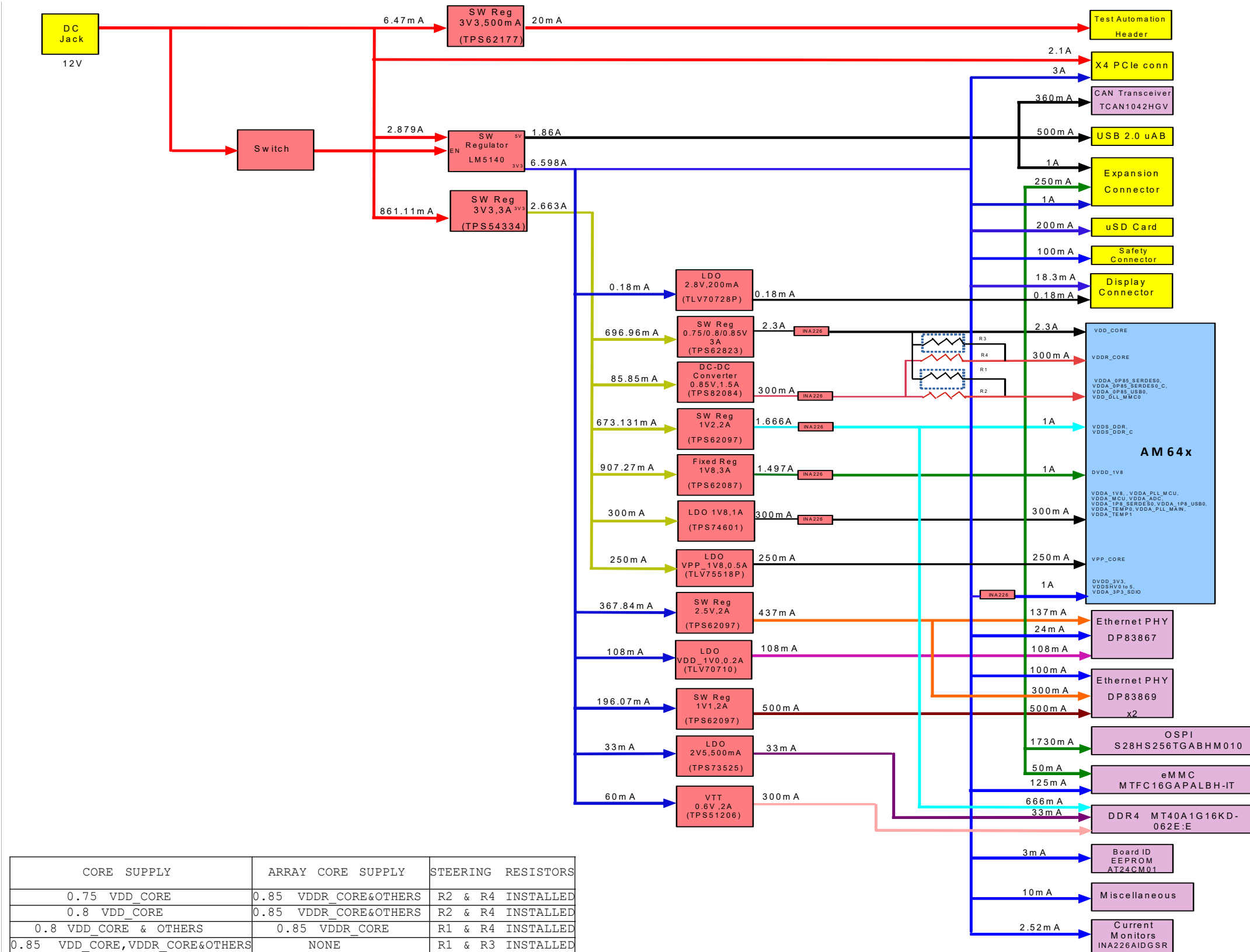
Title BLOCK DIAGRAM_CP BOARD

Size	Rev
C	D
Variant Name = PROC101D(004) TMDs64EVM	
Date: Monday, November 27, 2023	Sheet 3 of 40

BLOCK DIAGRAM_XDS110

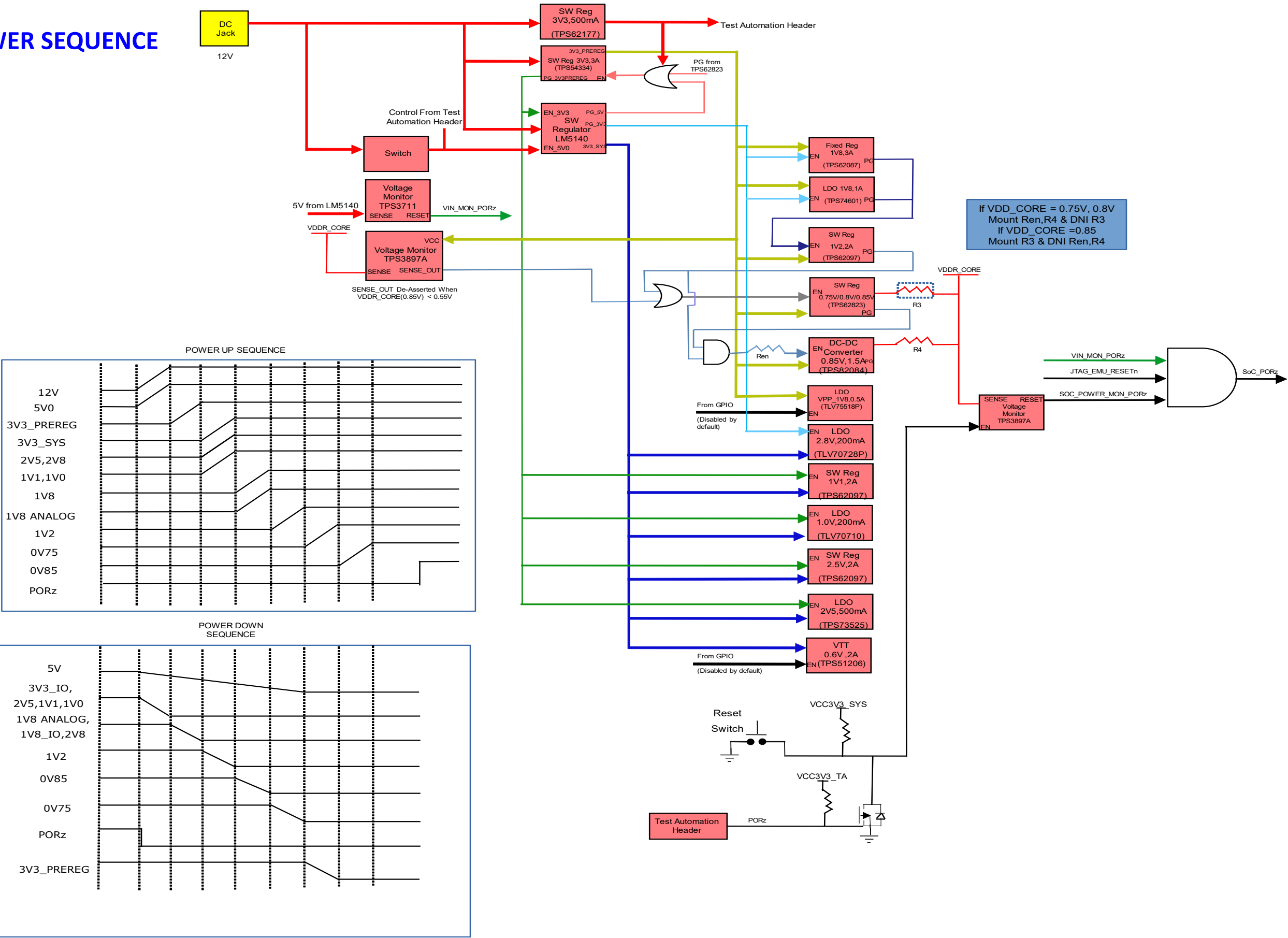


POWER FLOW DIAGRAM



CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

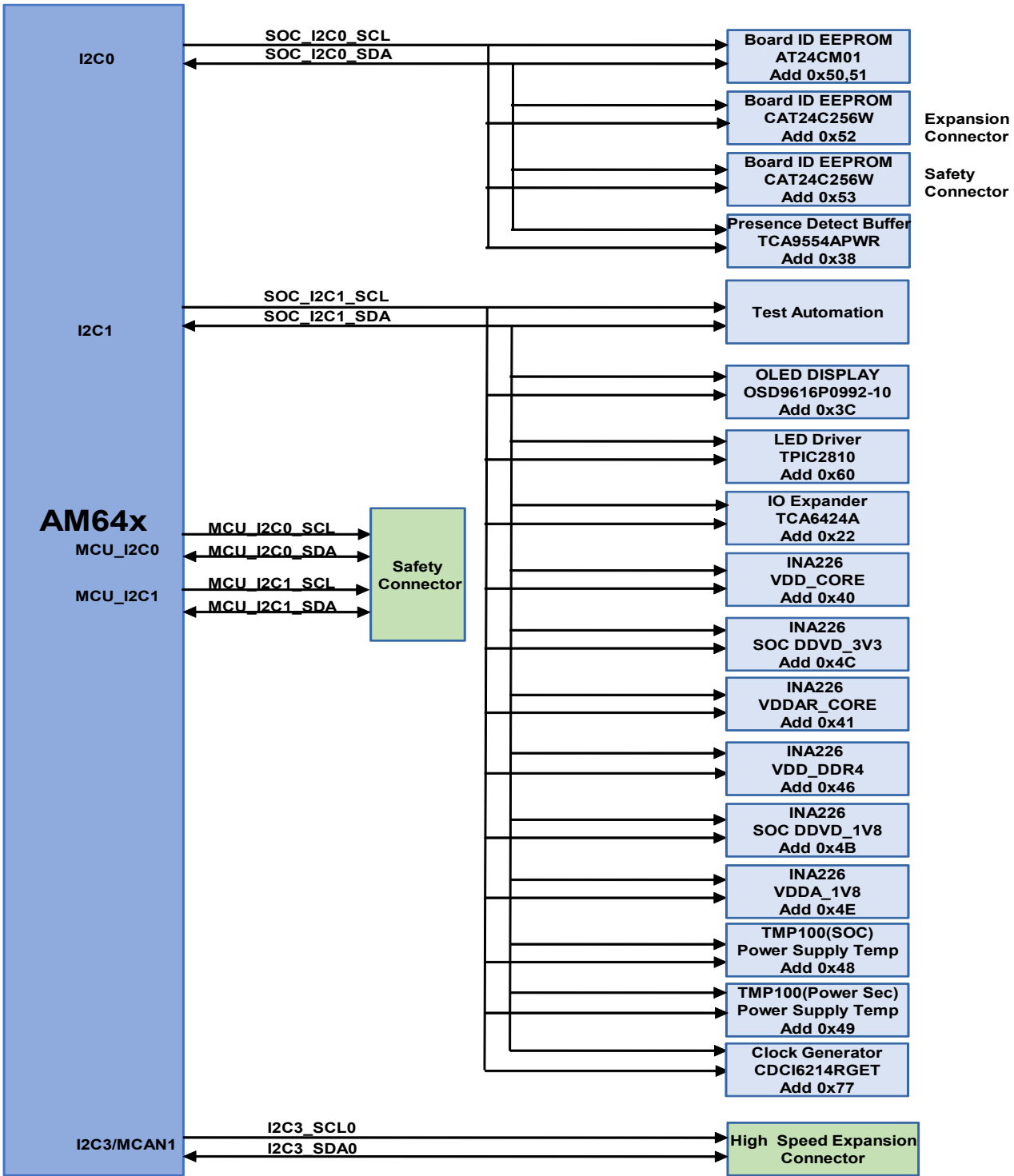
POWER SEQUENCE



GPIO MAPPING TABLE

S.NO	GPIO DESCRIPTION	GPIO NETNAME	REQUIRED ON	FUNCTIONALITY	GPIO USED	SoC Muxed Signal Name	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE
1	EMMC RESET Control GPIO	GPIO_eMMC_RSTn	GP EVM	Reset	IO EXPANDER- P00		OUTPUT	HIGH	LOW
2	OSPI RESET Control GPIO	GPIO_OSPI_RSTn	GP EVM	Reset	GPIO013	OSPI0_CS2	OUTPUT	HIGH	LOW
3	CPSW RGMII1 RESET Control GPIO	GPIO_CPSW1_RST	GP EVM	Reset	IO EXPANDER- P02		OUTPUT	HIGH	LOW
4	PRG1 RGMII1 Ethernet PHY RESET Control GPIO	GPIO_RGMII1_RST	GP EVM	Reset	IO EXPANDER- P03		OUTPUT	HIGH	LOW
5	PRG1 RGMII2 Ethernet PHY RESET Control GPIO	GPIO_RGMII2_RST	GP EVM	Reset	IO EXPANDER- P04		OUTPUT	HIGH	LOW
6	PRG1 RGMII1 Ethernet PHY Link Detection GPIO	PRG1_ETH1_LED_LINK	GP EVM	Link Detection	PRG1_PRU0_GPO8		INPUT	LOW	HIGH
7	PRG1 RGMII2 Ethernet PHY Link Detection GPIO	PRG1_ETH2_LED_LINK	GP EVM	Link Detection	PRG1_PRU1_GPO8		INPUT	LOW	HIGH
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	GP EVM	Interrupt	Connected to PRG1_RGMII_INT via 0E res		INPUT	HIGH	LOW
9	PRG1 Ethernet PHY 1Interrupt	PRG1_RGMII_INT	GP EVM	Interrupt	GPIO1_70	EXTINTn	INPUT	HIGH	LOW
10	PRG1 Ethernet PHY 2Interrupt			Interrupt			INPUT	HIGH	LOW
11	PCIe RESET Control GPIO	GPIO_PCIe_RST_OUT	GP EVM	Reset	IO EXPANDER- P05		OUTPUT	LOW	HIGH
12	SD card load switch enable control	MMC1_SD_EN	GP EVM	Load SW Enable	IO EXPANDER- P06		OUTPUT	HIGH	LOW
13	One GPIO is required to control the Mux select between HSE and FSI Connector	FSI_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P07		OUTPUT	PREFERABLE	PREFERABLE
14	One GPIO is required to enable Standby mode in CAN tranceiver	MCAN0_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P10		OUTPUT	LOW	HIGH
15	One GPIO is required to enable Standby mode in CAN tranceiver	MCAN1_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P11		OUTPUT	LOW	HIGH
16	One GPIO is required to control the Mux select between HSE and Ethernet PHY	CPSW_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P12		OUTPUT	PREFERABLE	PREFERABLE
17	MDC/MDIO FET Switch Select for Mux	PRG1_RGMII2_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P14		OUTPUT	PREFERABLE	PREFERABLE
18	VTT 0.6V regulator Enable	VTT_EN	GP EVM	VTT 0.6V regulator Enable	GPIO0_12	OSPI0_CSn1	OUTPUT	LOW	HIGH
19	TEST GPIO1 from Test Automation Connector/ GPIO for GP board push button	TEST GPIO1/GPIO1_43	GP EVM	GPIO for communications with AM64x	GPIO1_43	SPI0_CS1	INPUT	HIGH	LOW
20	TEST GPIO2 from Test Automation Connector	TEST GPIO2	GP EVM	GPIO for communications with AM64x	IO EXPANDER- P15		INPUT	HIGH	LOW
21	OLED Display RESET GPIO	GPIO_OLED_RESETn	GP EVM	Reset	IO EXPANDER- P16		OUTPUT	LOW	HIGH
22	IO Expander Interrupt	IO_EXP_INTn	GP EVM	Interrupt	GPIO1_78	MMC1_SDWP	INPUT	HIGH	LOW
23	VPP 1.8V regulator Enable	VPP_LDO_EN	GP EVM	VPP 01.8V regulator Enable	IO EXPANDER- P17		OUTPUT	LOW	HIGH
24	One GPIO is required to control the Mux select between HSE and CAN Interface	CAN_MUX_SEL	GP EVM	Mux Selection	IO EXPANDER- P01		OUTPUT	LOW	HIGH
25	User LED	TEST_LED1	GP EVM	Test	IO EXPANDER- P20		OUTPUT	LOW	HIGH
26	User LED	TEST_LED2	GP EVM	Test	MCU_SPI1_CS0	MCU_GPIO0_5	OUTPUT	LOW	HIGH
27	One GPIO to enable the PCIe Clock generator outputs	CDC_OE1/E4	GP EVM	Clock output enable	IO EXPANDER- P21		OUTPUT	HIGH	HIGH

I2C TREE

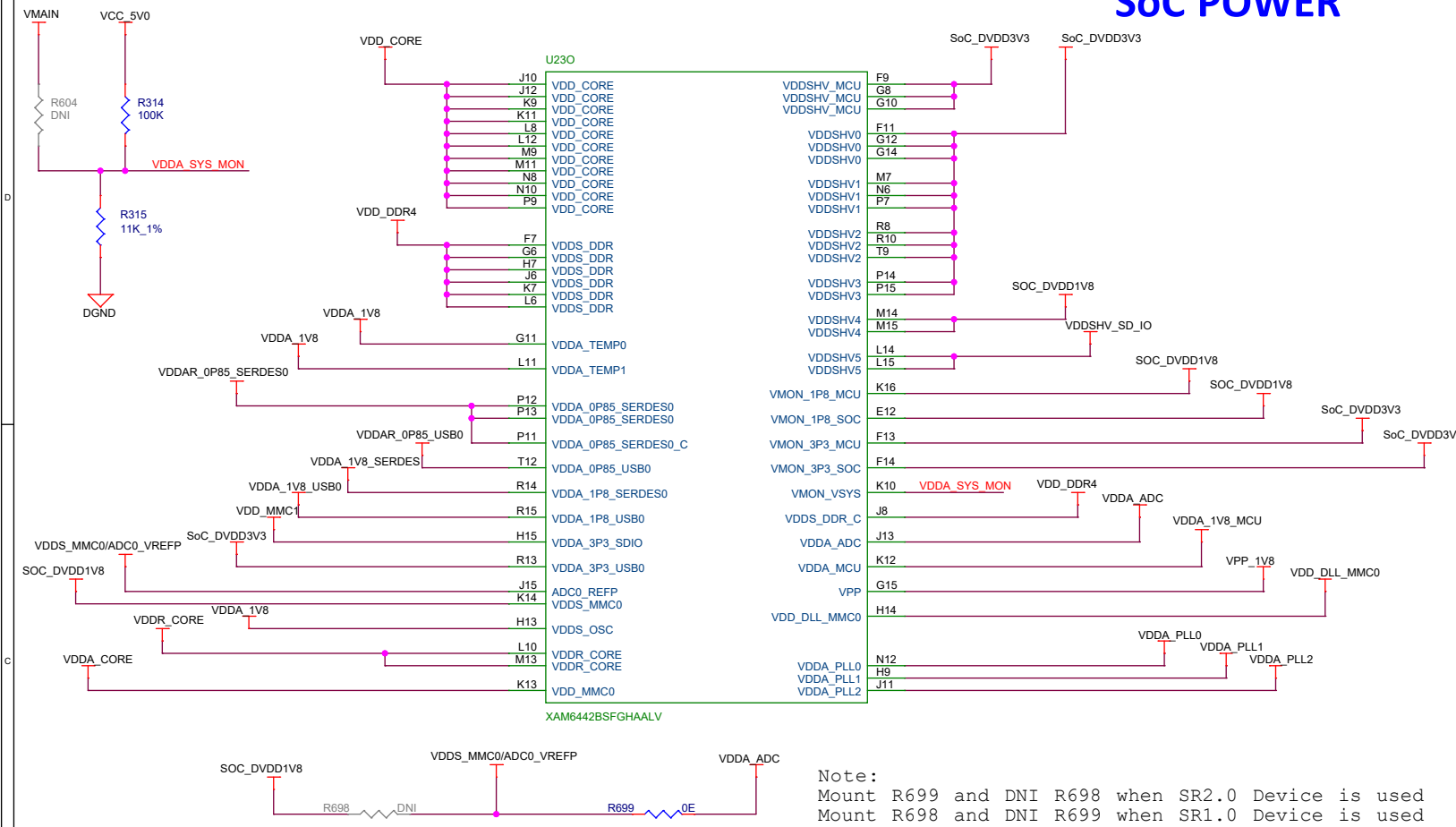


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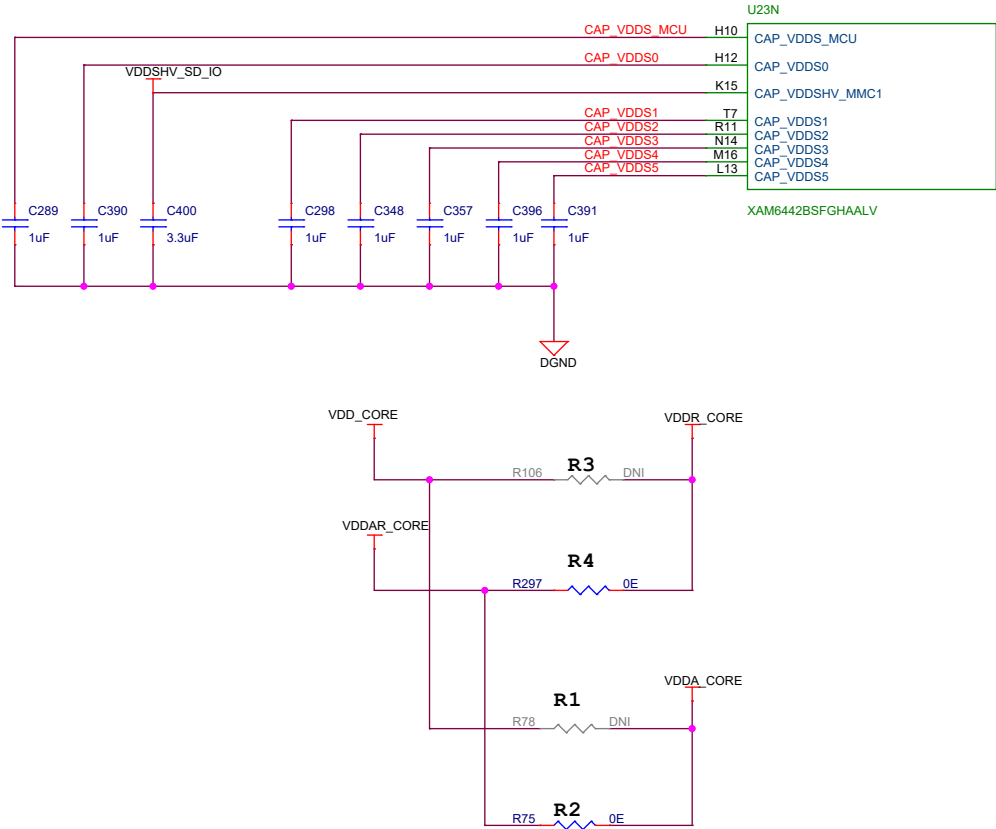
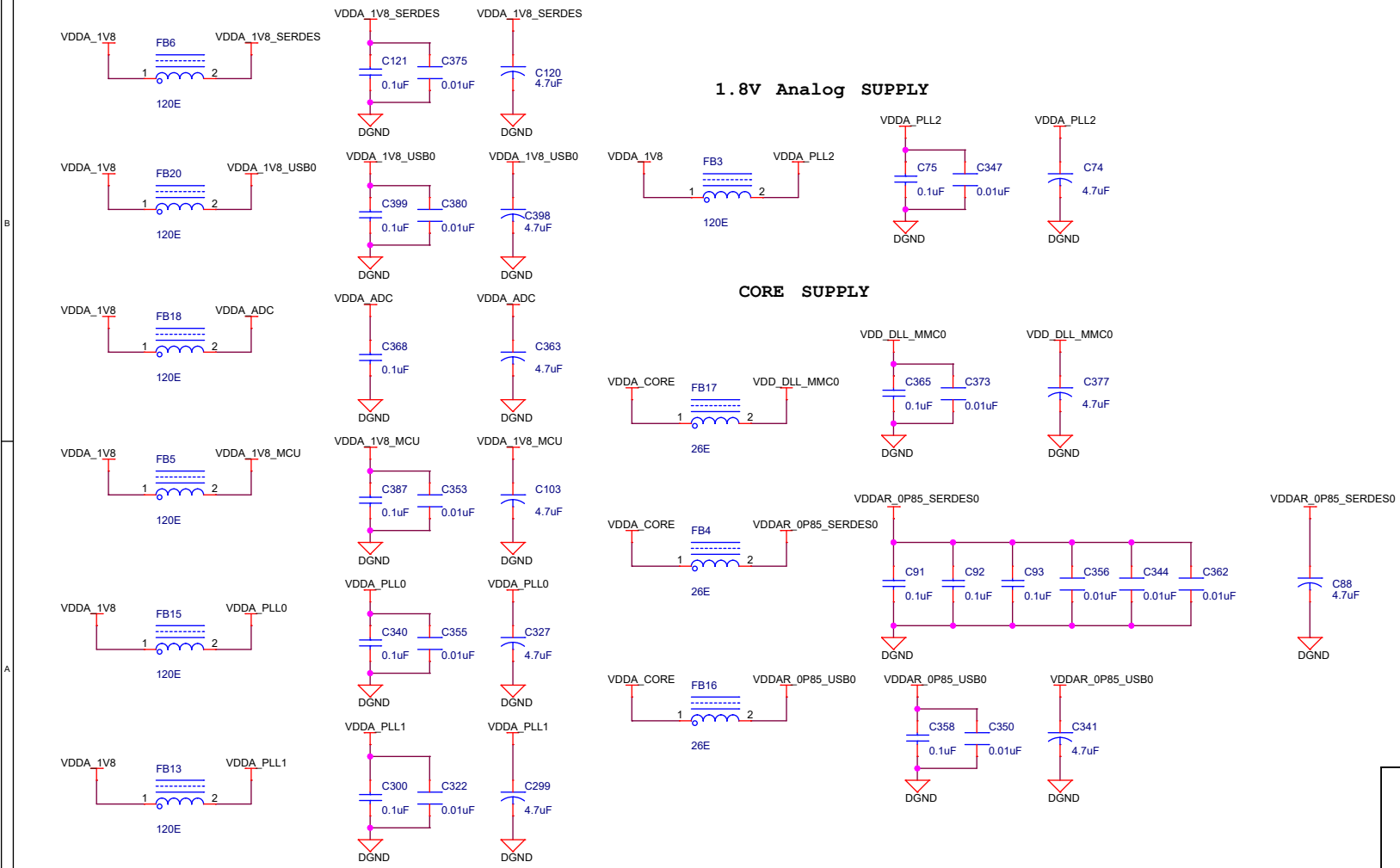
Title I2C TREE		
Size	Variant Name = PROC101D(004) TMDS64EVM	Rev
C		D
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SoC POWER



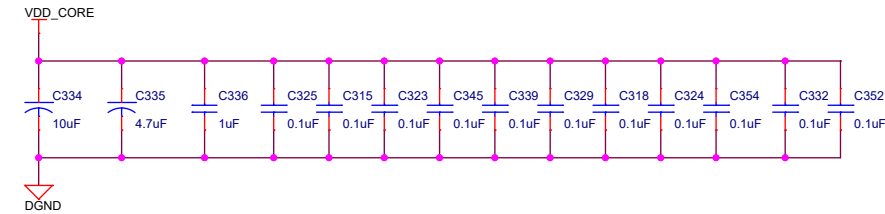
Note:
Mount R699 and DNI R698 when SR2.0 Device is used
Mount R698 and DNI R699 when SR1.0 Device is used

1.8V Analog SUPPLY

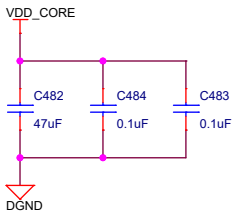


CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE, VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

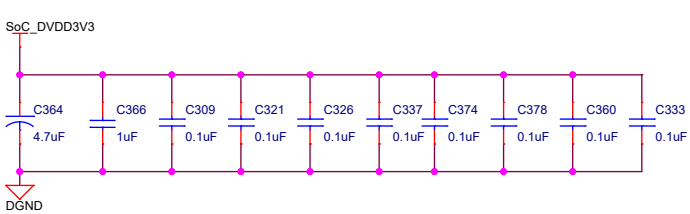
SoC POWER Decaps



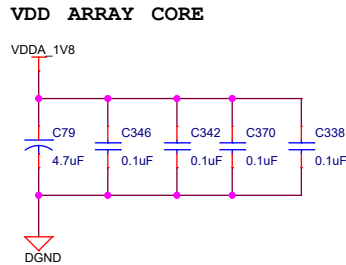
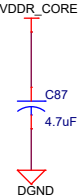
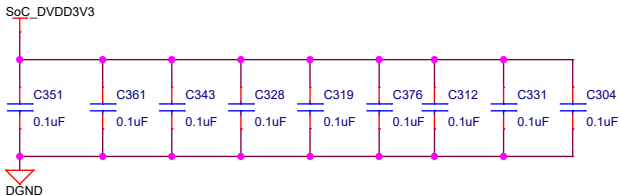
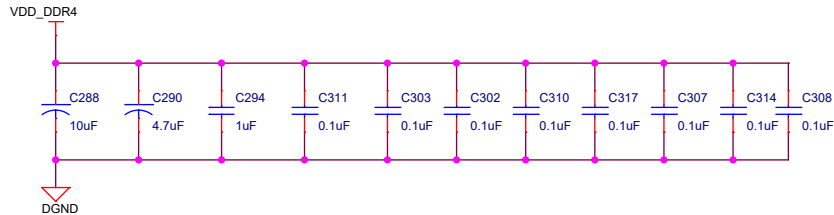
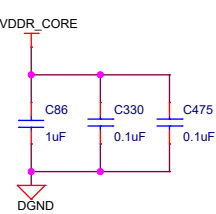
Place one 0.1uF cap near each Pin



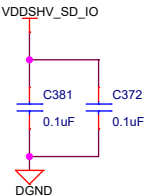
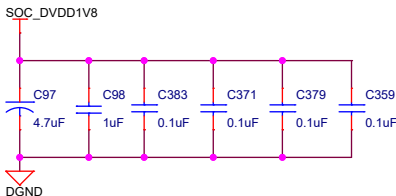
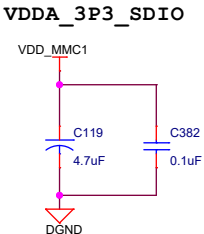
To place after current sense resitor on VDD_CORE plane



Place one 0.1uF cap near each Pin

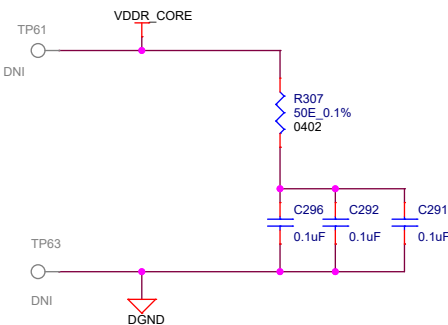
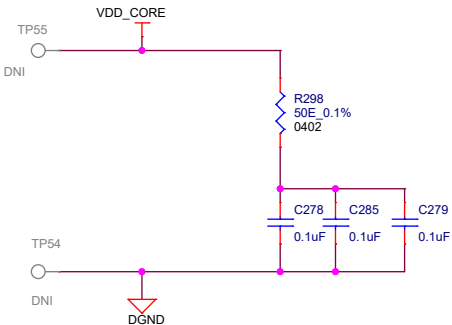


Place one 0.1uF cap near each Pin



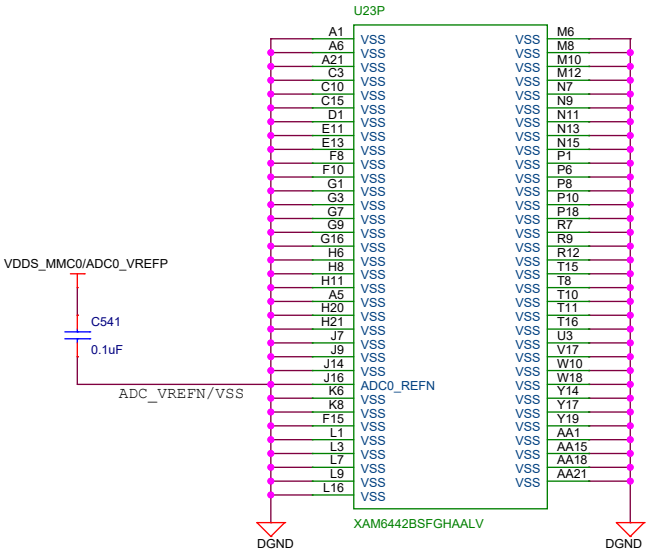
Place one 0.1uF cap near each Pin

Core & Array Core Supply Kelvin Sensing

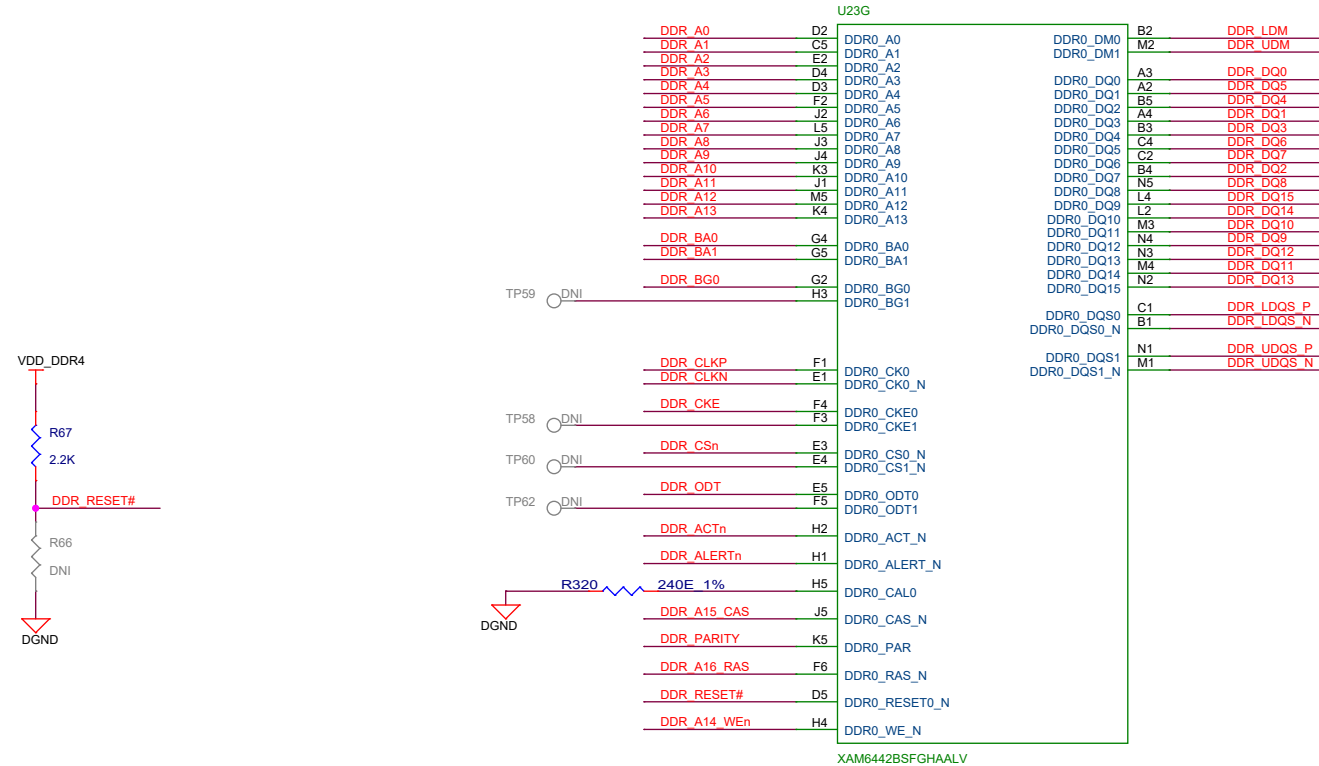


SoC POWER - VSS

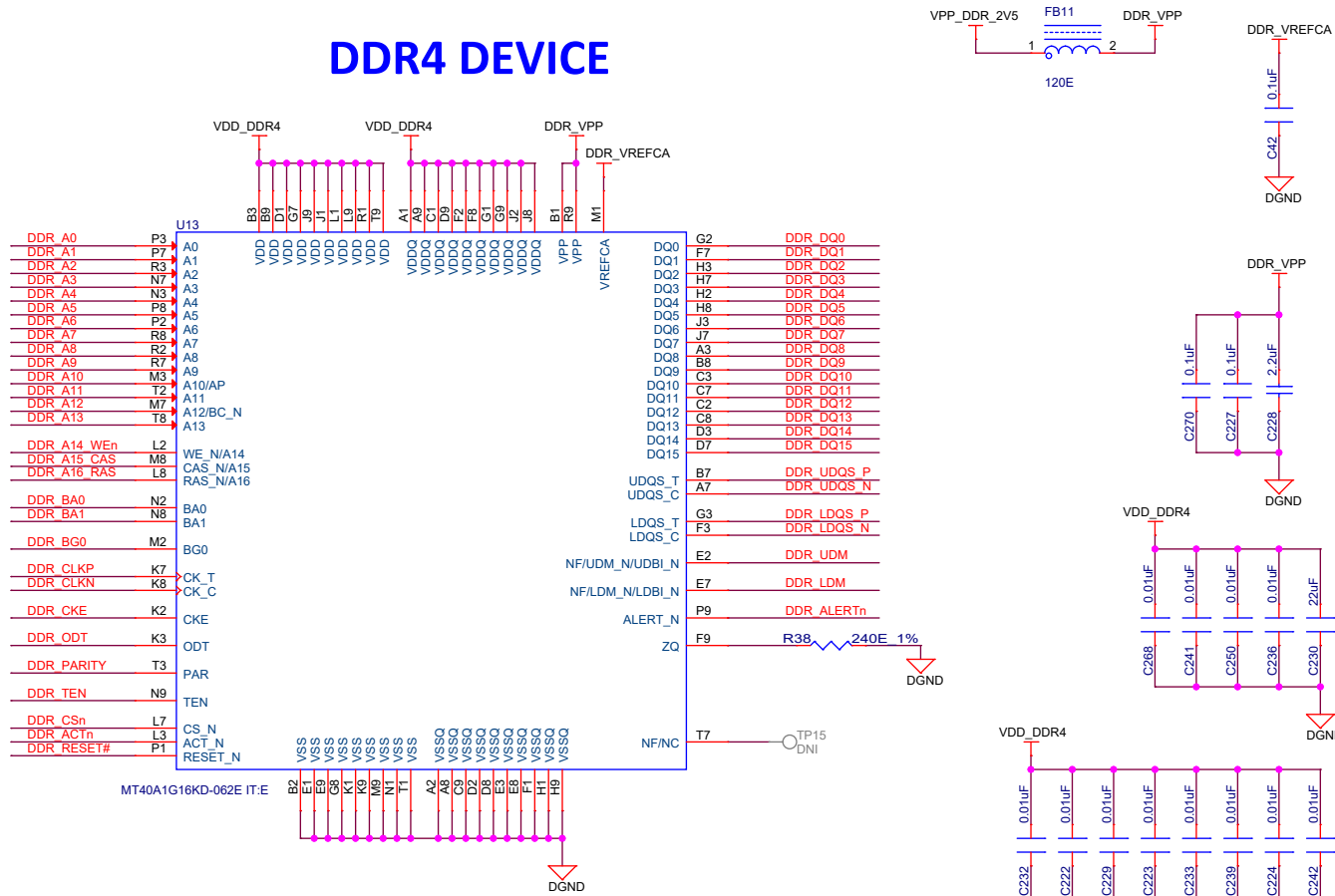
CAD Note:
Place CAP C541
between pins
J15 and J16



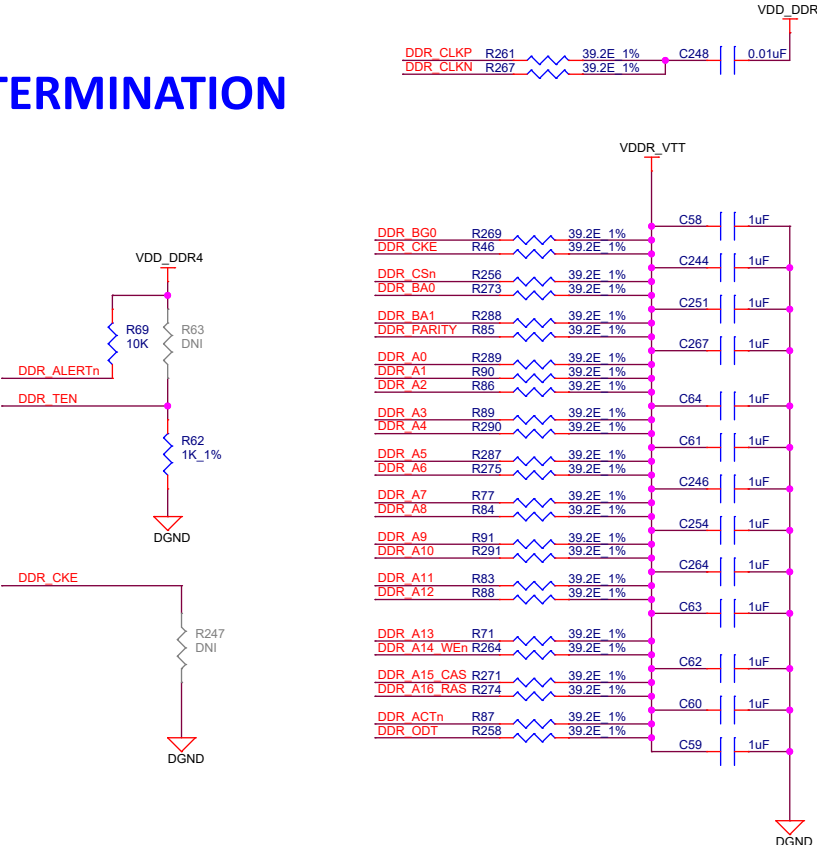
SoC DDR INTERFACE

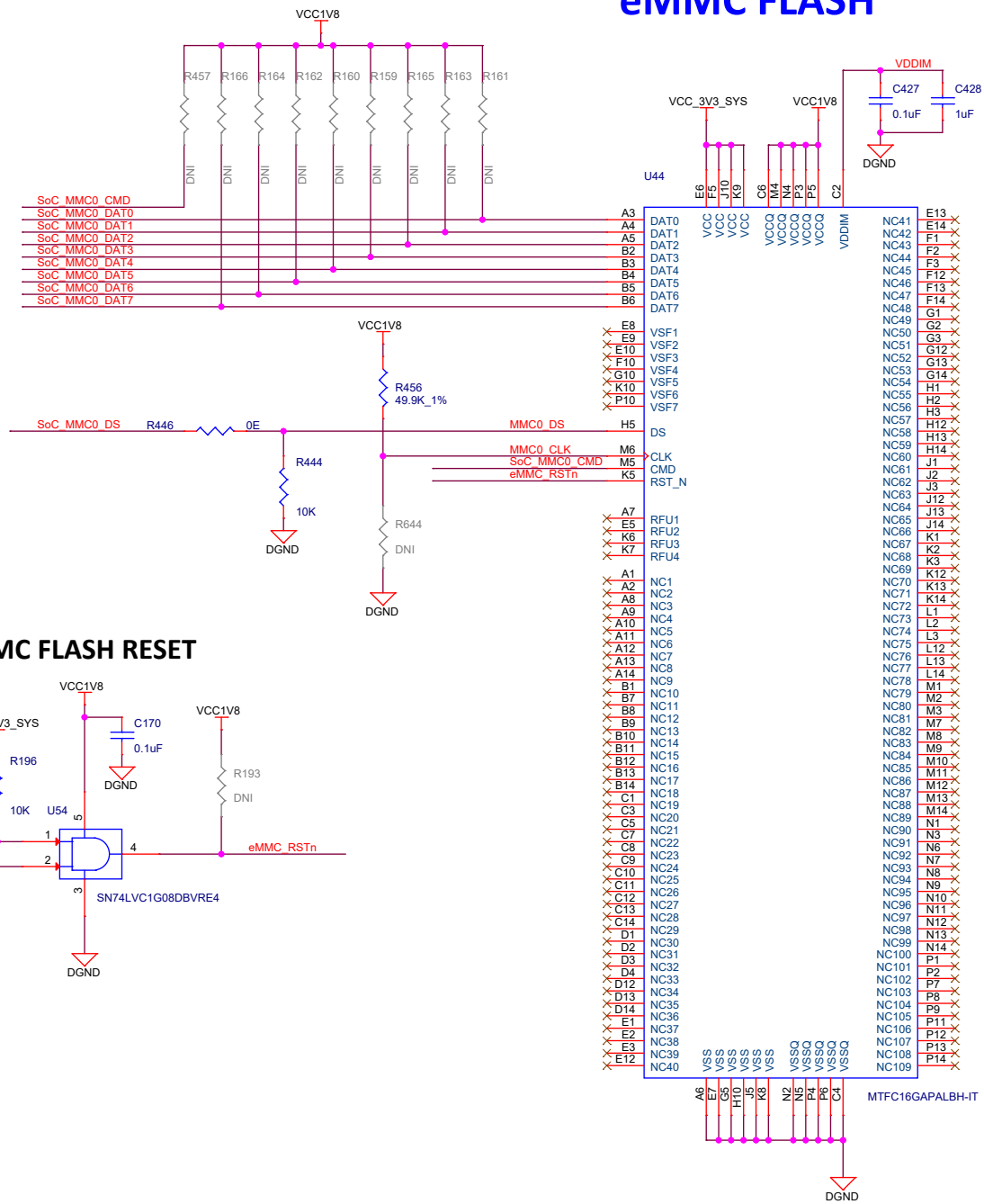
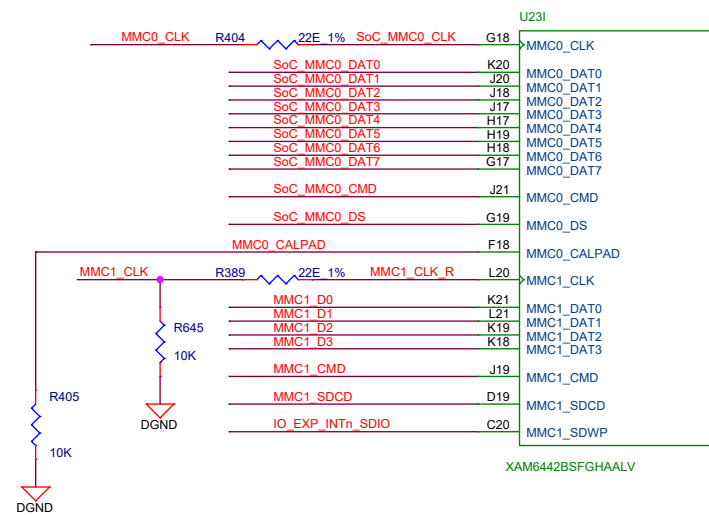


DDR4 DEVICE

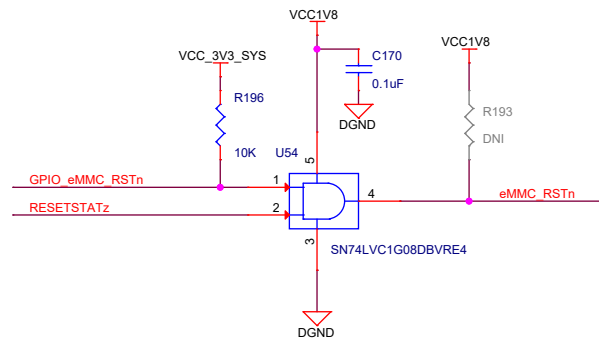


DDR TERMINATION

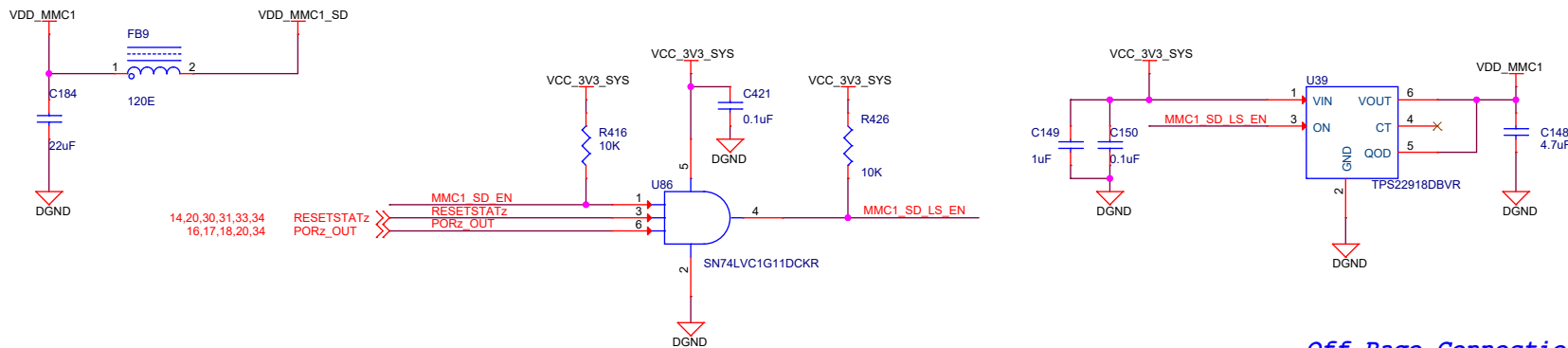
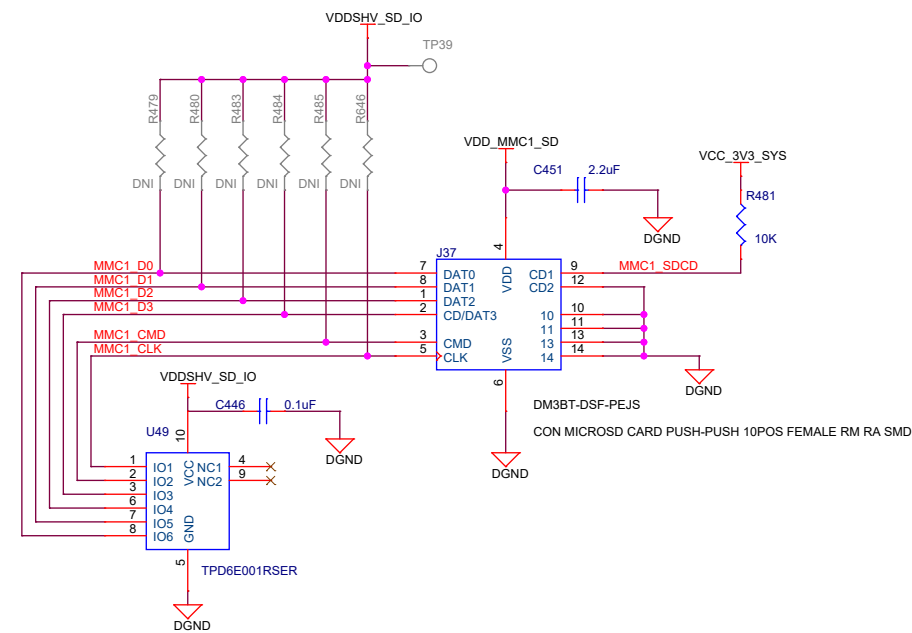




eMMC FLASH RESET



SD CARD INTERFACE



Off Page Connections

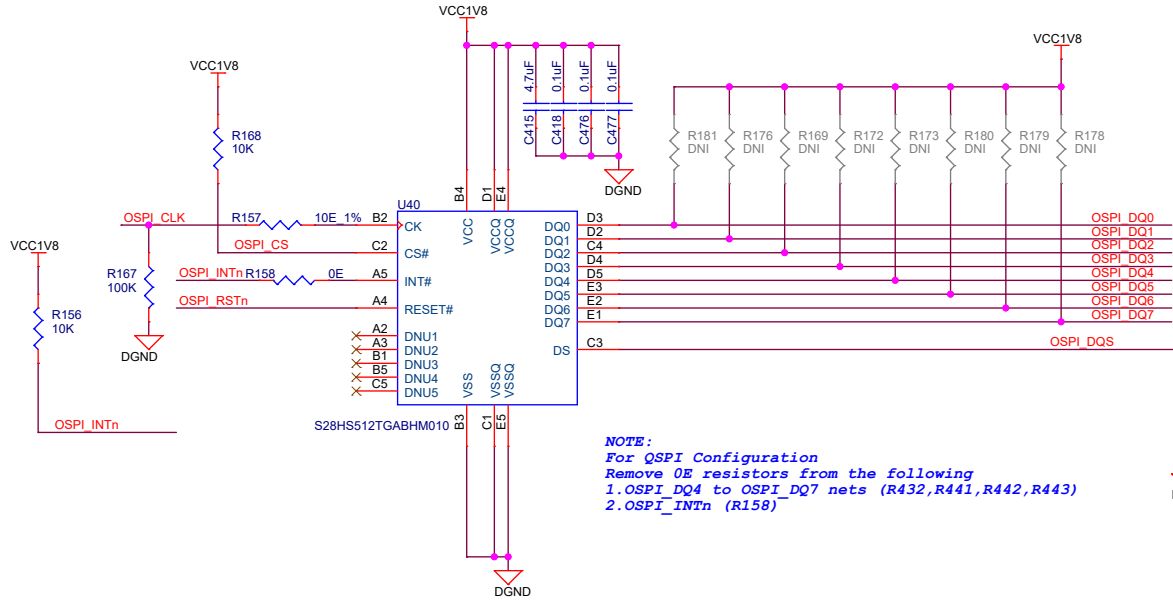
From 4	33	IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO
To IO Expander	33	GPIO_eMMC_RSTn	GPIO_eMMC_RSTn
	33	MMC1_SD_EN	MMC1_SD_EN

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Title eMMC FLASH_SDCARD INTERFACE		
Size	Variant Name = PROC101D(004) TMDs64EVM	Rev
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OSPI FLASH

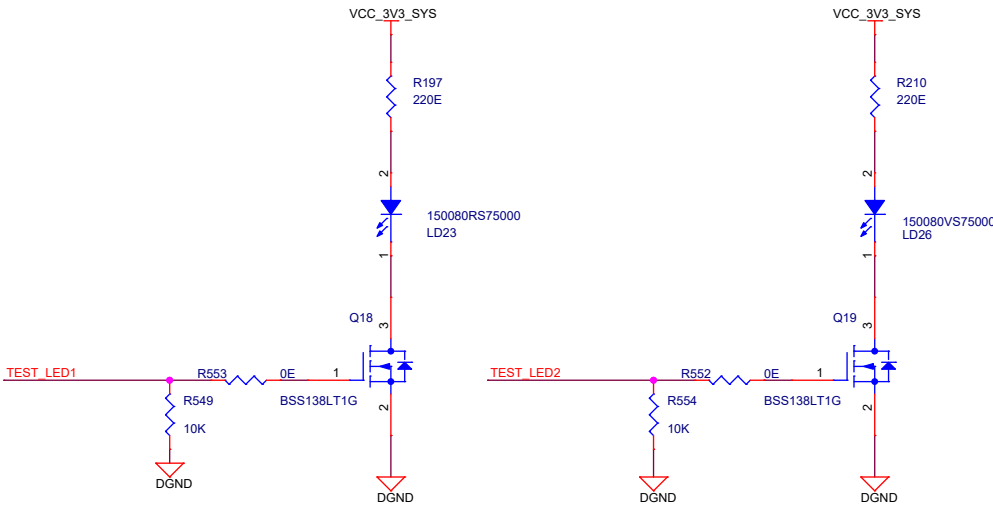


SOC OSPI INTERFACE

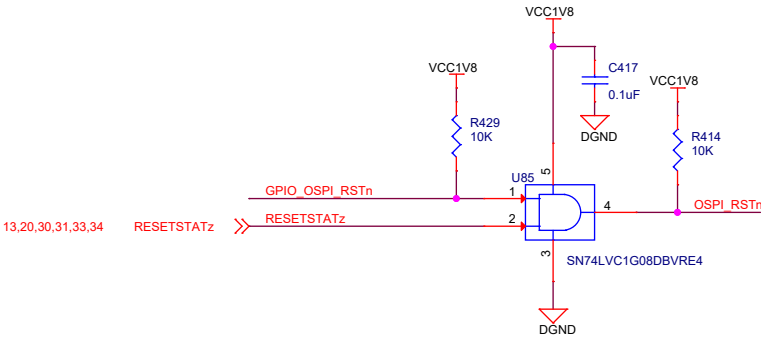


To Route DQS to LBCLK0	To Route DQS to SOC's DQS
Mount R591 & R600	Mount R601 & R592
DNI R601 & R592	DNI R591 & R600

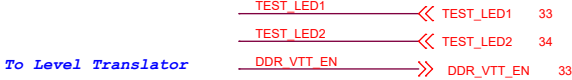
USER TEST LED



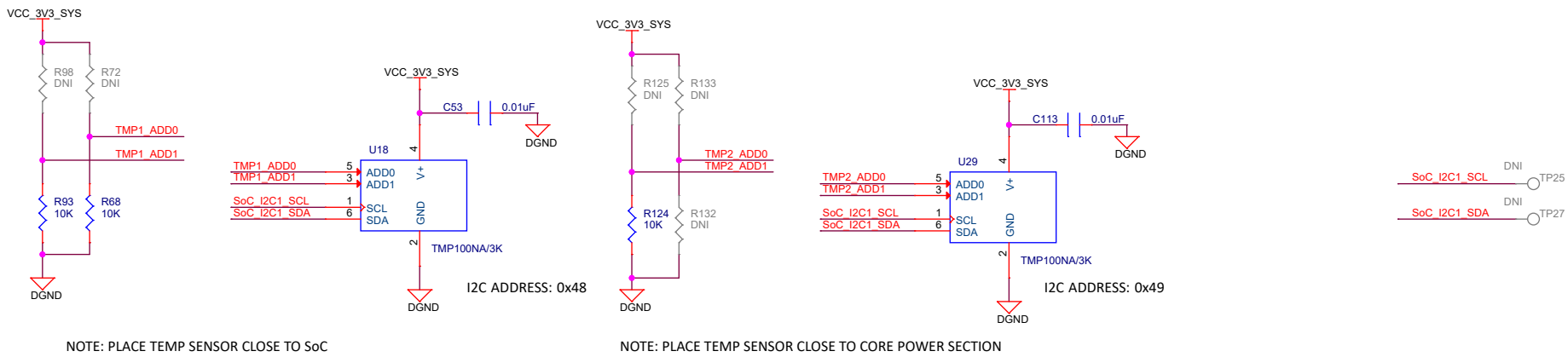
OSPI FLASH RESET



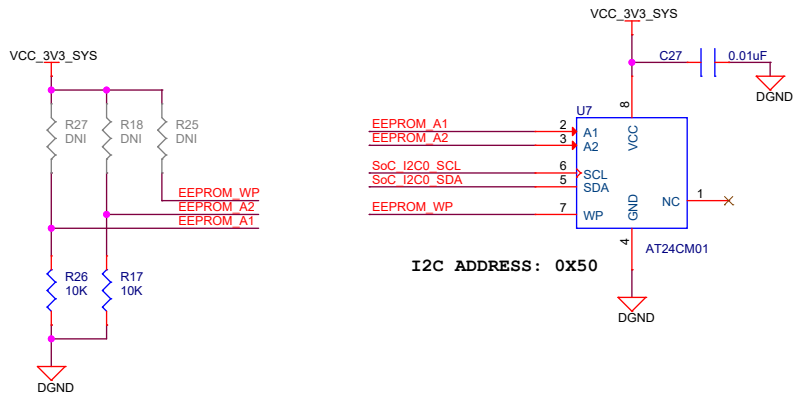
Off Page Connections



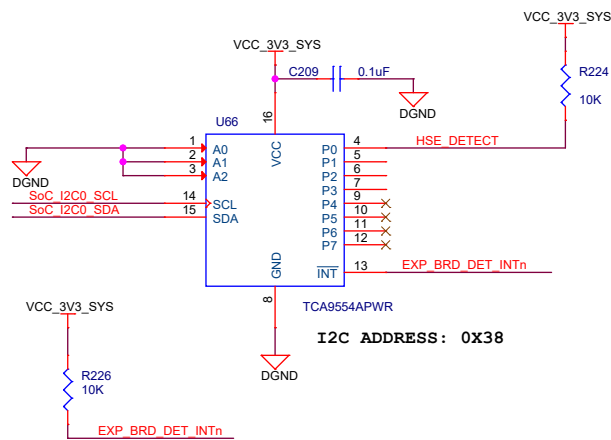
TEMPERATURE SENSOR



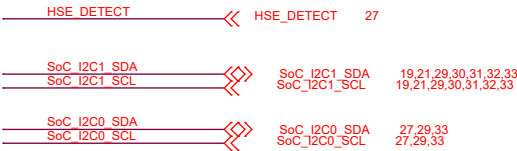
BOARD ID EEPROM



BOARD PRESENCE DETECT CIRCUIT



Off Page Connections



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Title EEPROM,PRESENCE DETECTION & TEMP SENSOR

Size Variant Name = PROC101D(004) TMDS64EVM

Date: Monday, November 27, 2023

Sheet 15 of 40

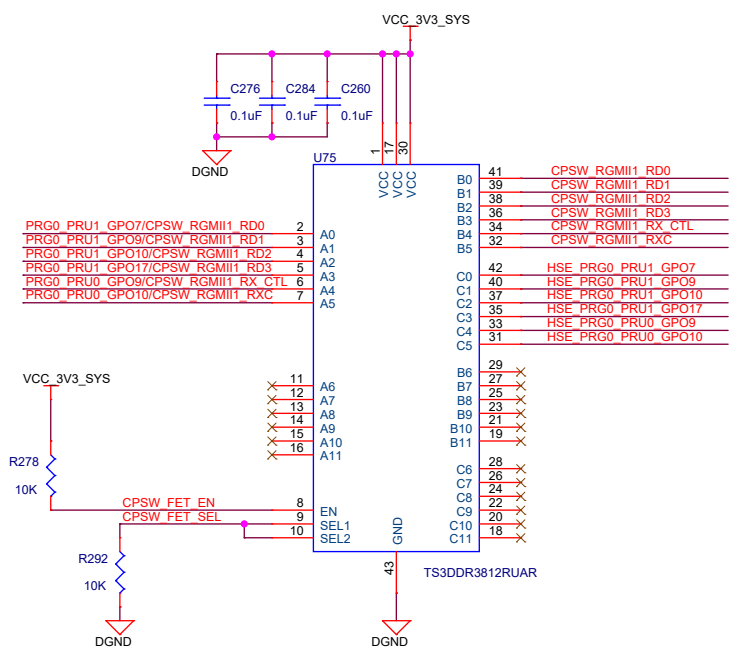
Rev D

The image displays three circuit diagrams illustrating the placement of decoupling capacitors for different power rails:

- VDD_1V0:** A series of capacitors (C51, C39, C41, C36, C259, C253, C274, C238) connected to the VDD_1V0 rail and ground (DGND). The capacitors C51, C39, C41, C36, C259, C253, and C274 are 1uF, while C238 and C263 are 10uF.
- VCC_3V3_SYS:** A series of capacitors (C275, C44, C35, C52, C266, C237, C281) connected to the VCC_3V3_SYS rail and ground (DGND). The capacitors C275, C44, C35, C52, C266, and C237 are 1uF, while C281 is 10uF.
- VDD_2V5:** A series of capacitors (C38, C43, C249, C261, C258) connected to the VDD_2V5 rail and ground (DGND). The capacitors C38, C43, C249, and C261 are 1uF, while C258 is 10uF.

The diagram illustrates a 3V3 supply network. The input VCC_3V3_SYS is connected to a network of resistors and diodes. The resistors are labeled R56, R51, R39, R32, R33, R41, R35, R54, R52, R249, R31, R34, R251, and R36. The diodes are labeled DNI. The network is connected to a GND symbol.

CPSW RGMII 1 ETHERNET PHY SIGNALS & HSE CON SIGNALS



EN	SEL1	SEL2	FUNCTION
L	X	X	A0 to A11, B0 to B11, and C0 to C11 are Hi-Z
H	L	L	A0 to A5 = B0 to B5 and A6 to A11 = B6 to B11
H	L	H	A0 to A5 = B0 to B5 and A6 to A11 = C6 to C11
H	H	L	A0 to A5 = C0 to C5 and A6 to A11 = B6 to B11
H	H	H	A0 to A5 = C0 to C5 and A6 to A11 = C6 to C11

[illegible]

From					
Processor	27	PRG0_PRU1_GPO7/CPSW_RGMII1_RD0	»	CPSW_RGMII1_RD0	
	27	PRG0_PRU1_GPO9/CPSW_RGMII1_RD1	»	CPSW_RGMII1_RD1	
	27	PRG0_PRU1_GPO10/CPSW_RGMII1_RD2	»	CPSW_RGMII1_RD2	
	27	PRG0_PRU1_GPO17/CPSW_RGMII1_RD3	»	CPSW_RGMII1_RD3	
	27	PRG0_PRU0_GPO9/CPSW_RGMII1_RX_CTL	»	PRG0_PRU0_GPO9/CPSW_RGMII1_RX_CTL	
	27	PRG0_PRU0_GPO10/CPSW_RGMII1_RXC	»	PRG0_PRU0_GPO10/CPSW_RGMII1_RXC	
From Processor	27	CPSW_RGMII1_TD0	»	CPSW_RGMII1_TD0	
	27	CPSW_RGMII1_TD1	»	CPSW_RGMII1_TD1	
	27	CPSW_RGMII1_TD2	»	CPSW_RGMII1_TD2	
	27	CPSW_RGMII1_TD3	»	CPSW_RGMII1_TD3	
	27	CPSW_RGMII1_TX_CTL	»	CPSW_RGMII1_TX_CTL	
	27	CPSW_RGMII1_TXC	»	CPSW_RGMII1_TXC	
	13,17,18,20,34	PORz_OUT	»	PORz_OUT	
	17,18,34	PRG1_RGMII1_INTn	»	PRG1_RGMII1_INTn	
From IO Expander	16,33	GPIO_CPSW1_RST	»	GPIO_CPSW1_RST	
	33	CPSW_FET_SEL	»	CPSW_FET_SEL	
From Clock Buffer	31	CPSW_RGMII1_ETH1_CLK	»	CPSW_RGMII1_ETH1_CLK	
To HSE Connector	27	HSE_PRG0_PRU1_GPO7	»	HSE_PRG0_PRU1_GPO7	
	27	HSE_PRG0_PRU1_GPO7	»	HSE_PRG0_PRU1_GPO9	
	27	HSE_PRG0_PRU1_GPO10	»	HSE_PRG0_PRU1_GPO10	
	27	HSE_PRG0_PRU1_GPO17	»	HSE_PRG0_PRU1_GPO17	
	27	HSE_PRG0_PRU0_GPO9	»	HSE_PRG0_PRU0_GPO10	
	27	HSE_PRG0_PRU0_GPO10	»	HSE_PRG0_PRU0_GPO10	
From Processor	17,27	CPSW_RGMII1_MDIO	»	CPSW_RGMII1_MDIO	
	17,27	CPSW_RGMII1_MDC	»	CPSW_RGMII1_MDC	



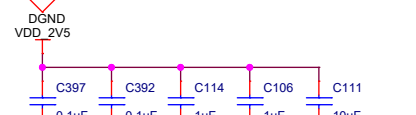
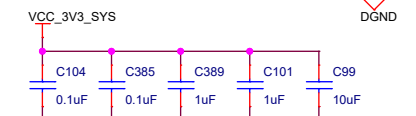
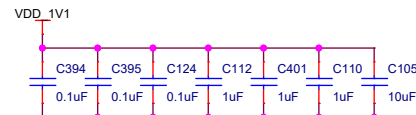
TEXAS
INSTRUMENTS



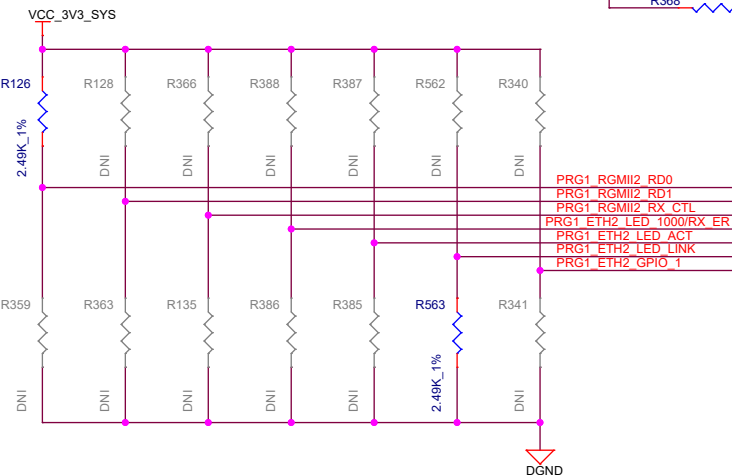
Size		
C	Variant Name = PROC101D(004) TMDS64EVM	
Date	Month	Year

Date: Monday, November 27, 2023	Sheet 16 of 40
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ICSSG1 - RGMII 2

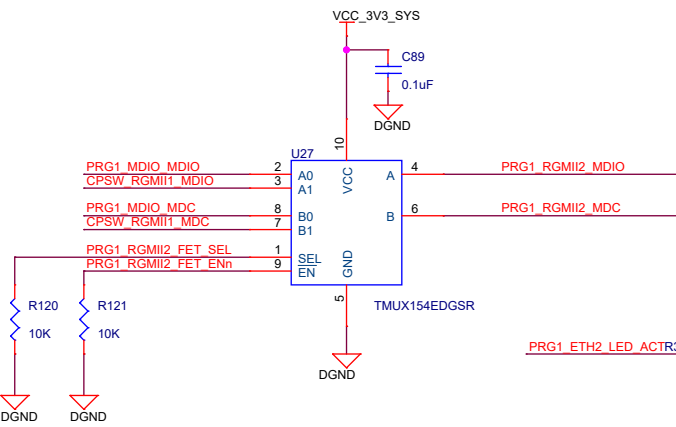


STRAPPING RESISTORS



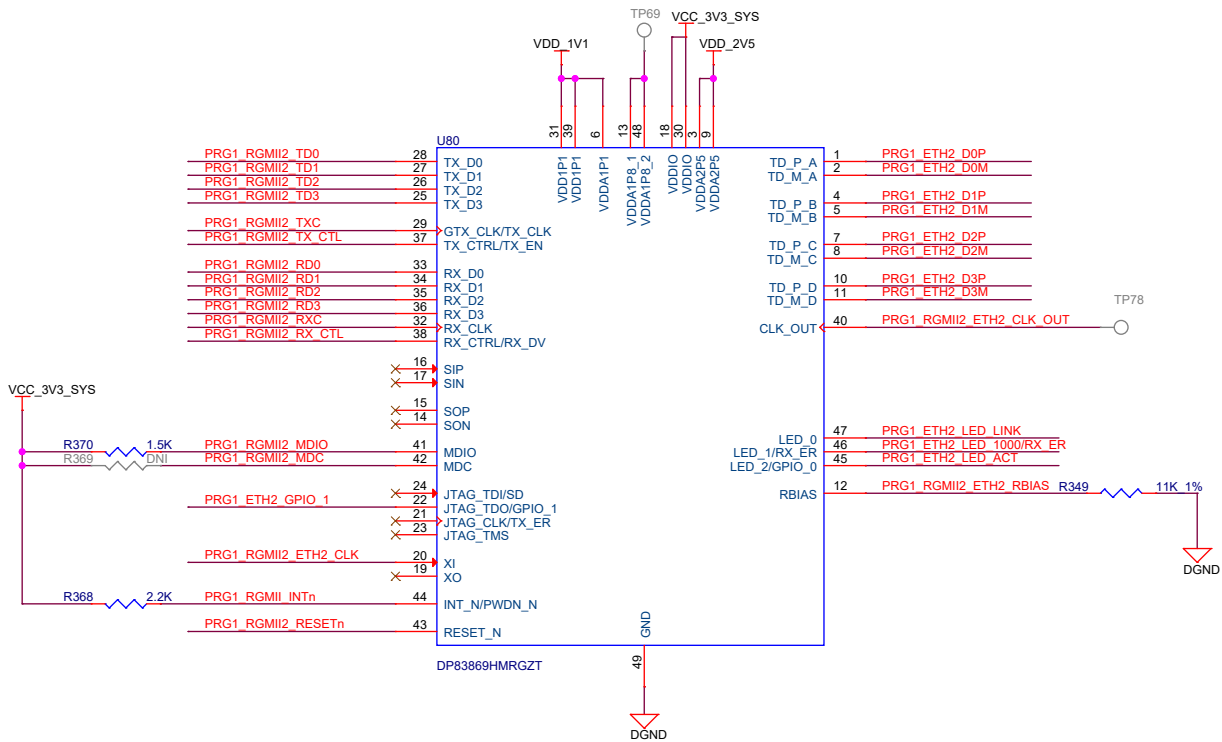
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PHY ADDRESS = 00011
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000BaseT/100Base-TX/10Base-T)
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PRG1 MDC/MDIO FET SWITCH

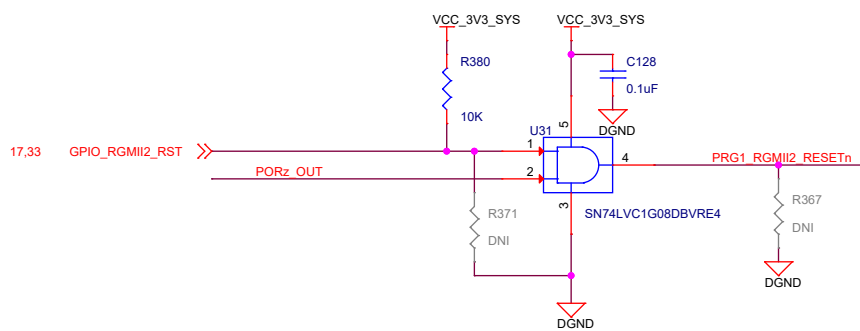


TMUX154EDGSR Truth Table

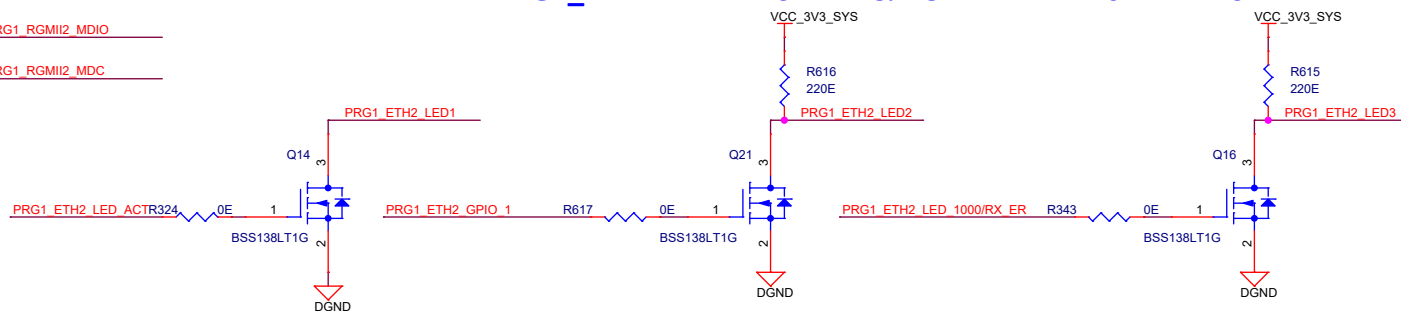
SEL	EN	FUNCTION
X	H	Disconnect
L	L	A = A0 B = B0
H	L	A = A1 B = B1



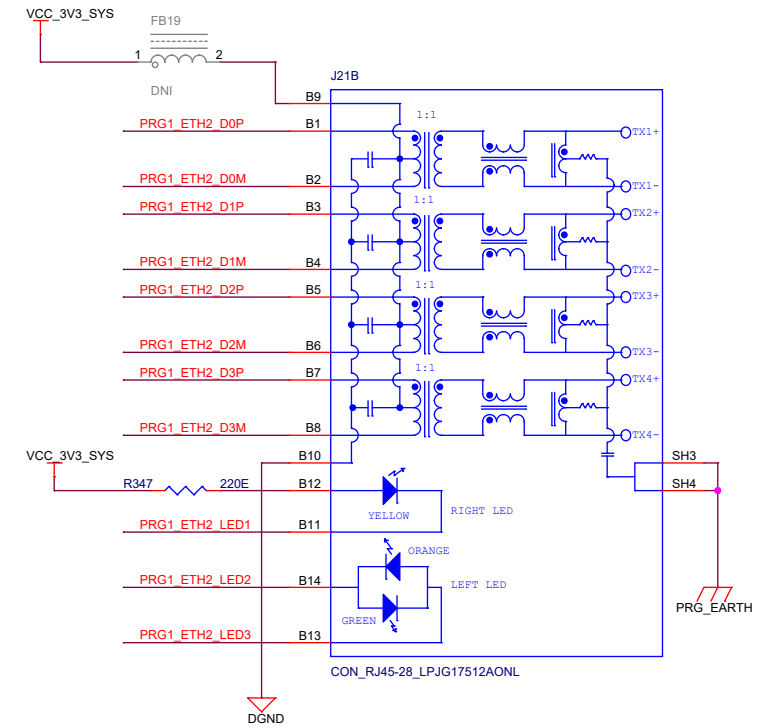
PRG1 ETH2 RESET



PRG1_ETHERNET - 2 SPEED & ACTIVITY LED 's DRIVERS



Dual RJ45 CON With Integrated Magnetics



Off Page Connections

To Processor	16,18,34	PRG1_RGMII_INTn	PRG1_RGMII_INTn
	27	PRG1_RGMII2_RD0	PRG1_RGMII2_RD0
	27	PRG1_RGMII2_RD1	PRG1_RGMII2_RD1
	27	PRG1_RGMII2_RD2	PRG1_RGMII2_RD2
	27	PRG1_RGMII2_RD3	PRG1_RGMII2_RD3
	27	PRG1_RGMII2_RXC	PRG1_RGMII2_RXC
	27	PRG1_RGMII2_RX_CTL	PRG1_RGMII2_RX_CTL
From Processor	27	PRG1_ETH2_LED_LINK	PRG1_ETH2_LED_LINK
	27	PRG1_ETH2_LED_1000/RX_ER	PRG1_ETH2_LED_1000/RX_ER
	27	PRG1_RGMII2_TD0	PRG1_RGMII2_TD0
	27	PRG1_RGMII2_TD1	PRG1_RGMII2_TD1
	27	PRG1_RGMII2_TD2	PRG1_RGMII2_TD2
	27	PRG1_RGMII2_TD3	PRG1_RGMII2_TD3
	27	PRG1_RGMII2_TXC	PRG1_RGMII2_TXC
From CPSW SW	13,16,18,20,34	PORz_OUT	PORz_OUT
	18,27	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	18,27	PRG1_MDIO_MDC	PRG1_MDIO_MDC
	16,27	CPSW_RGMII1_MDIO	CPSW_RGMII1_MDIO
	16,27	CPSW_RGMII1_MDC	CPSW_RGMII1_MDC
	17,33	GPIO_RGMII2_RST	GPIO_RGMII2_RST
	33	PRGT_RGMII2_FET_SEL	PRGT_RGMII2_FET_SEL
From IO Expander			
From Clock Buffer		31	PRG1_RGMII2_ETH2_CLK

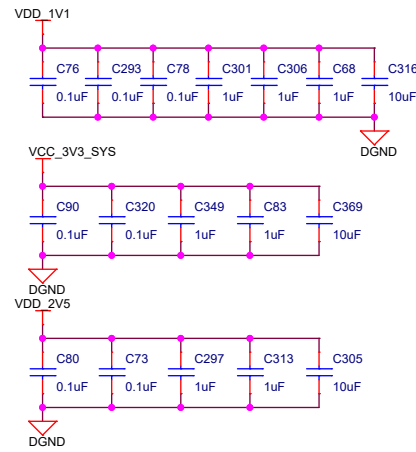
Designed for TI by Mistral Solutions Pvt Ltd



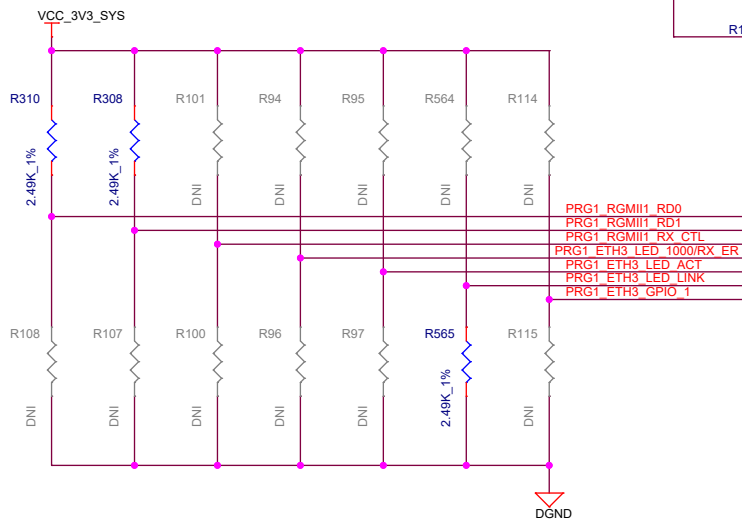
Title	ICSSG1 RGMII_2 ETHERNET PHY
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Size	Variant Name = PROC101D(004) TMSD64EVM	Rev
C		D
Date:	Monday, November 27, 2023	Sheet 17 of 40

Decaps

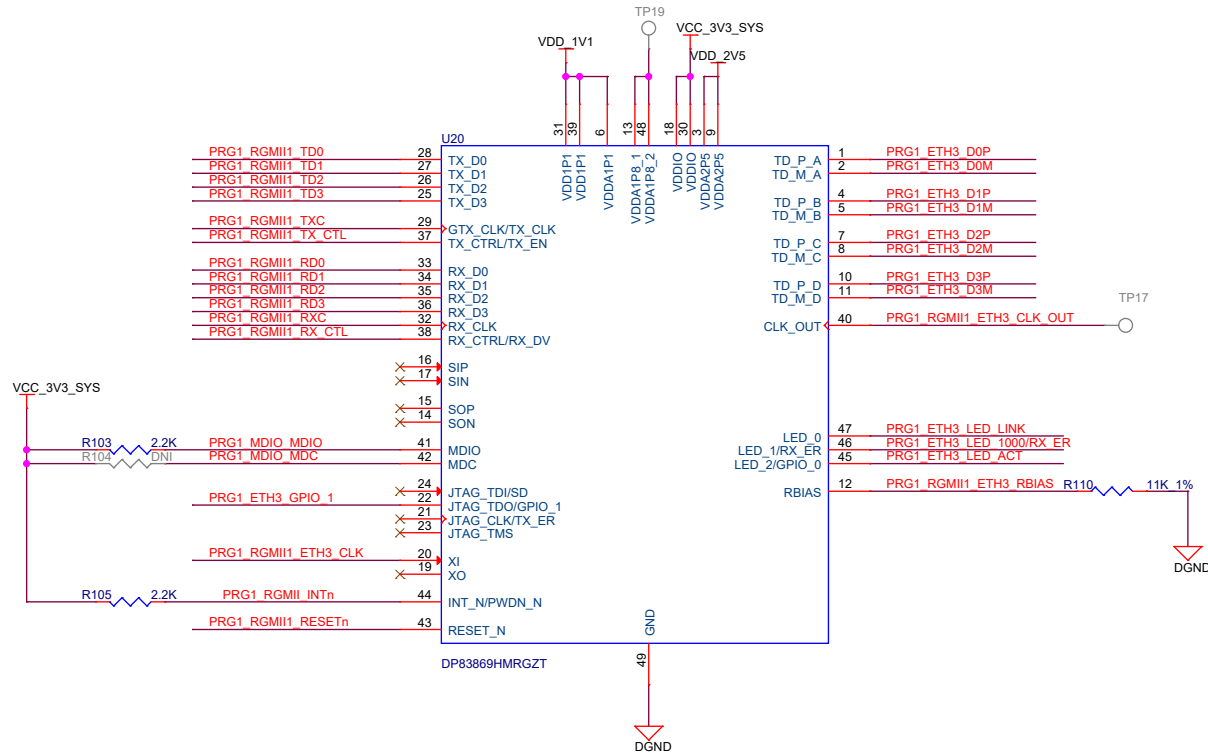


STRAPPING RESISTORS

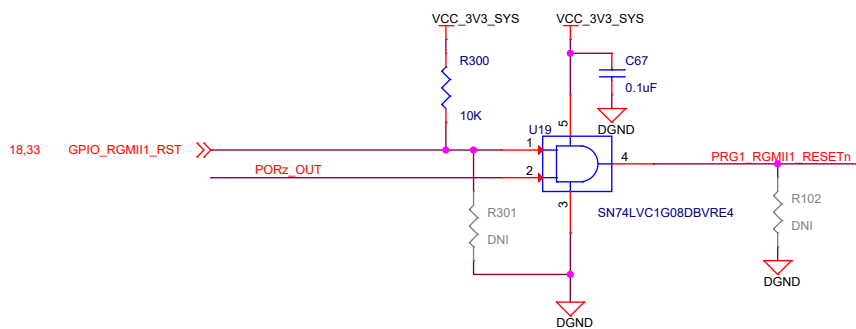


PHY ADDRESS = 01111
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000BaseT/100Base-TX/10Base-T)

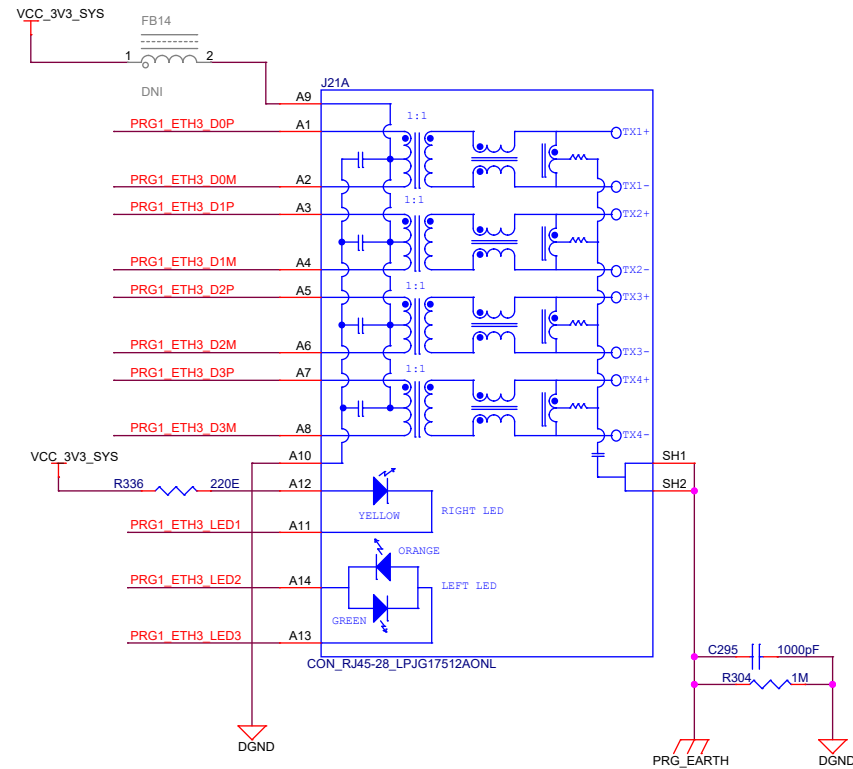
ICSSG1 - RGMII 1



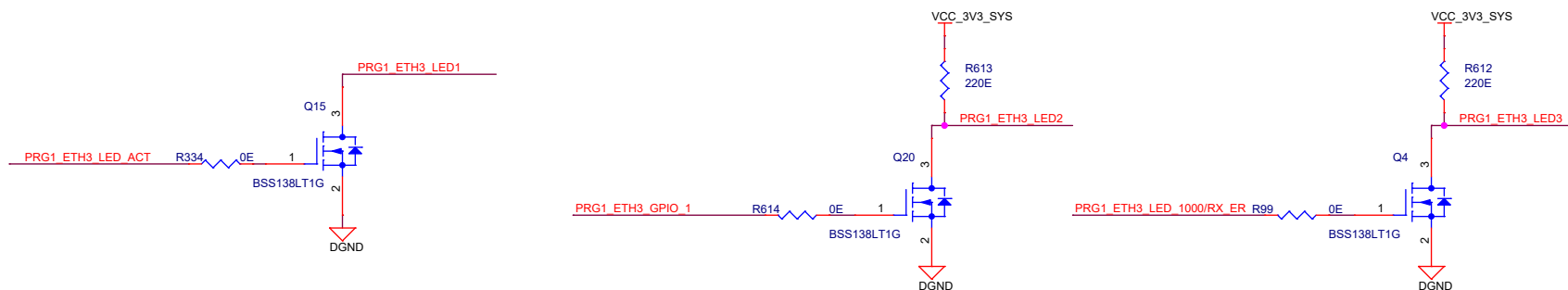
PRG1 ETH2 RESET



Dual RJ45 CON With Integrated Magnetics



PRG1_ETHERNET - 3 SPEED & ACTIVITY LED 's DRIVERS



Off Page Connections

To Processor	16,17,34	PRG1_RGMII1_INTn	PRG1_RGMII1_INTn
	27	PRG1_RGMII1_RD0	PRG1_RGMII1_RD0
From Processor	27	PRG1_RGMII1_RD1	PRG1_RGMII1_RD1
	27	PRG1_RGMII1_RD2	PRG1_RGMII1_RD2
From Processor	27	PRG1_RGMII1_RD3	PRG1_RGMII1_RD3
	27	PRG1_RGMII1_RXC	PRG1_RGMII1_RXC
From Processor	27	PRG1_RGMII1_RX_CTL	PRG1_RGMII1_RX_CTL
	27	PRG1_ETH3_LED_LINK	PRG1_ETH3_LED_LINK
From Processor	27	PRG1_ETH3_LED_1000/RX_ER	PRG1_ETH3_LED_1000/RX_ER
	27	PRG1_ETH3_LED_1000/RX_ER	PRG1_ETH3_LED_1000/RX_ER
From Processor	17,27	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	17,27	PRG1_MDIO_MDC	PRG1_MDIO_MDC
From IO Expander	18,33	GPIO_RGMII1_RST	GPIO_RGMII1_RST
	31	PRG1_RGMII1_ETH3_CLK	PRG1_RGMII1_ETH3_CLK

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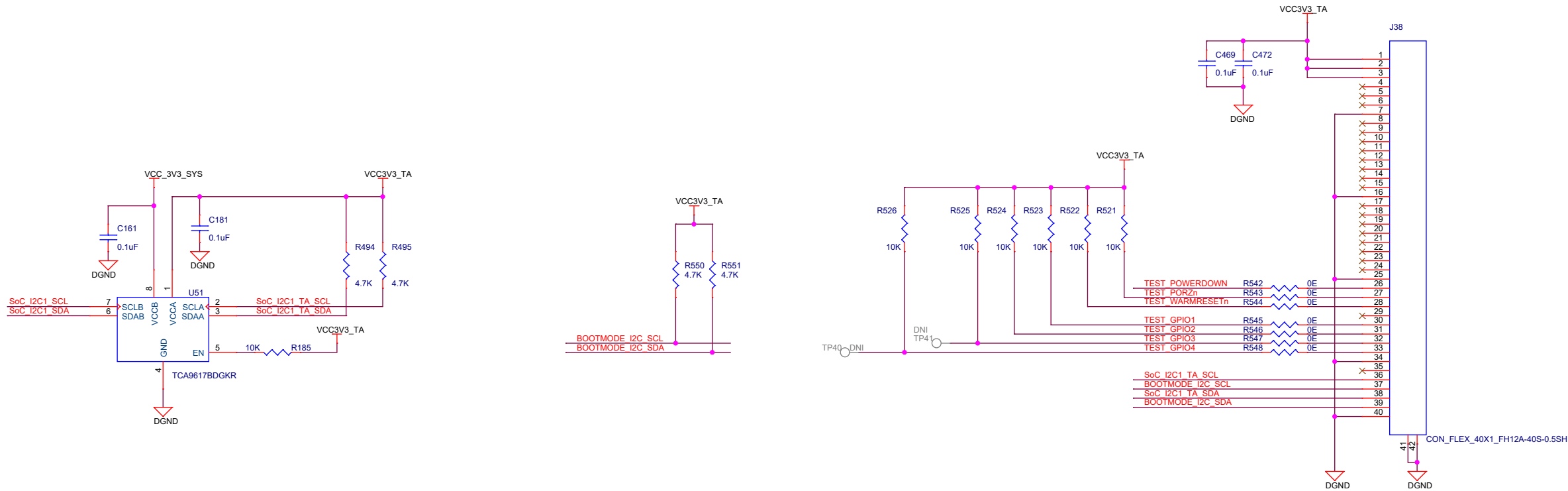


Title ICSSG2 RGMII_1 ETHERNET PHY

Size	Variant Name = PROC101D(004) TMDSS64EVM	Rev
C		D
Date:	Monday, November 27, 2023	Sheet 18 of 40

TEST AUTOMATION

40-PIN AUTOMATION HEADER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO0_13_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to I/O Expander to Communicate with SoC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

Off Page Connections

To Processor	15,21,29,30,31,32,33	SoC_I2C1_SCL SoC_I2C1_SDA	SoC_I2C1_SCL SoC_I2C1_SDA
To Bootmode Buffer	20	BOOTMODE_I2C_SCL BOOTMODE_I2C_SDA	BOOTMODE_I2C_SCL BOOTMODE_I2C_SDA
To Debounce Ckt	35	TEST_PORZn	TEST_PORZn
To High Side SW	37	TEST_POWERDOWN	TEST_POWERDOWN
To Debounce Ckt	35	TEST_WARMRESETn	TEST_WARMRESETn
To IO Expander	35	TEST_GPIO1	TEST_GPIO1
To EN Boot Mode Buffer	33	TEST_GPIO2	TEST_GPIO2
To RST Boot Mode Buffer	20	TEST_GPIO3	TEST_GPIO3
	20	TEST_GPIO4	TEST_GPIO4

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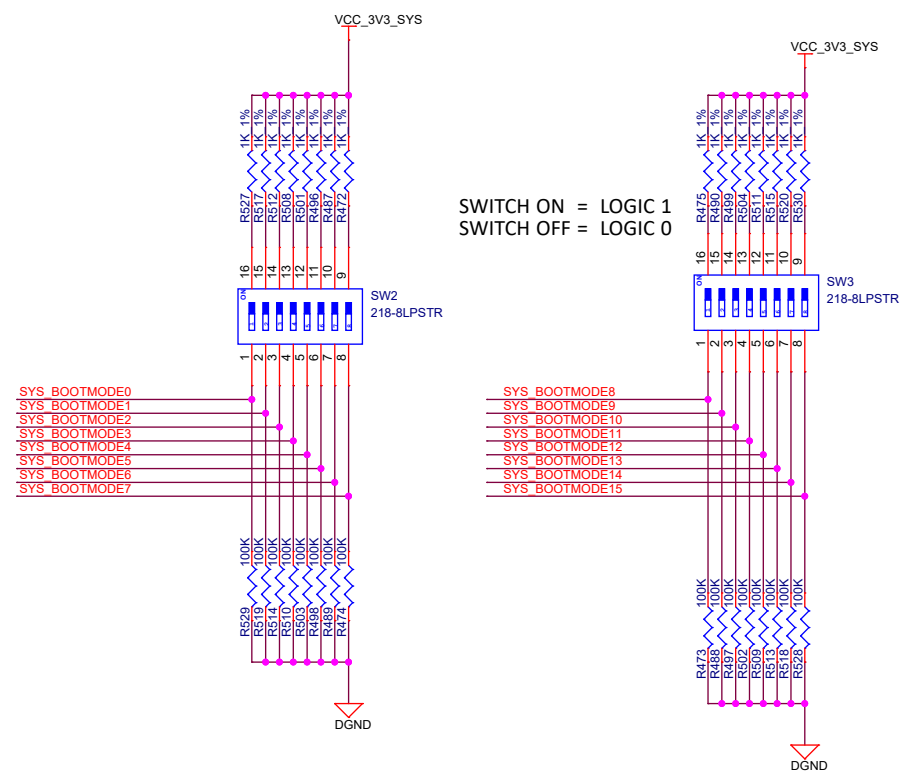
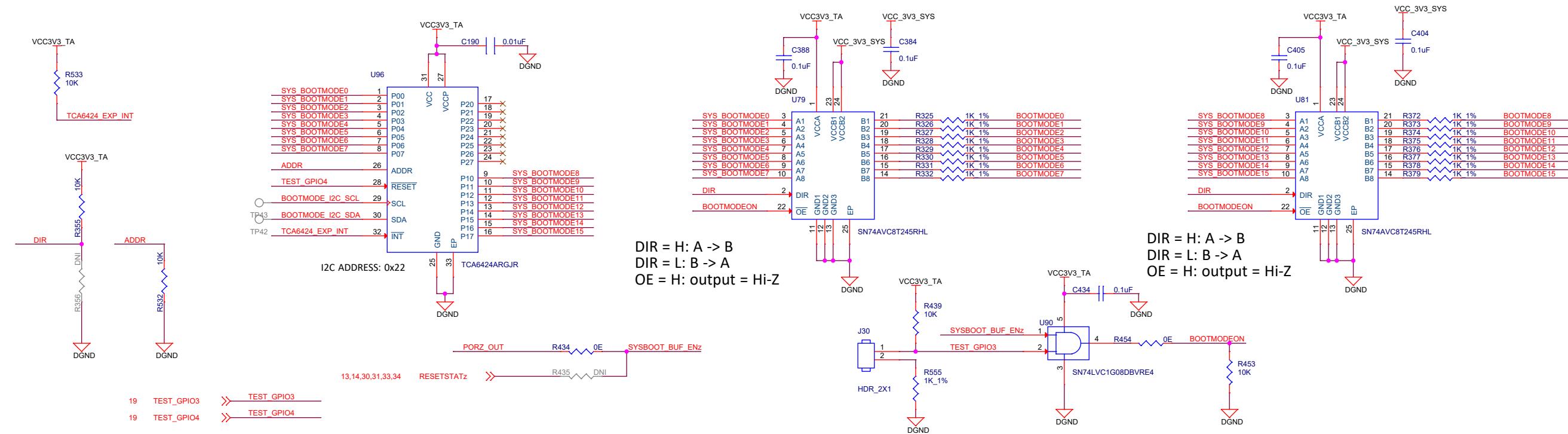
Title TEST AUTOMATION

Size
C Variant Name = PROC101D(004) TMDs64EVM

Rev
D

Date: Monday, November 27, 2023 Sheet 19 of 40

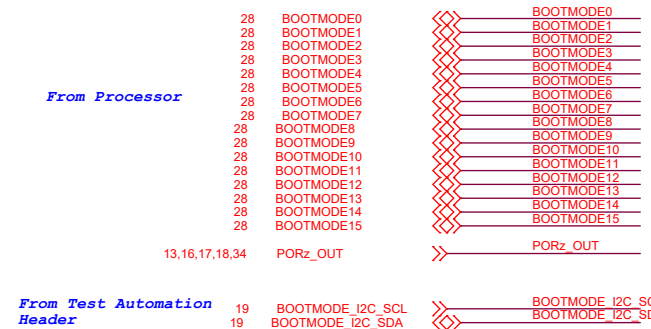
BOOT MODE BUFFER & SWITCHES



BOOT MODES SUPPORTED

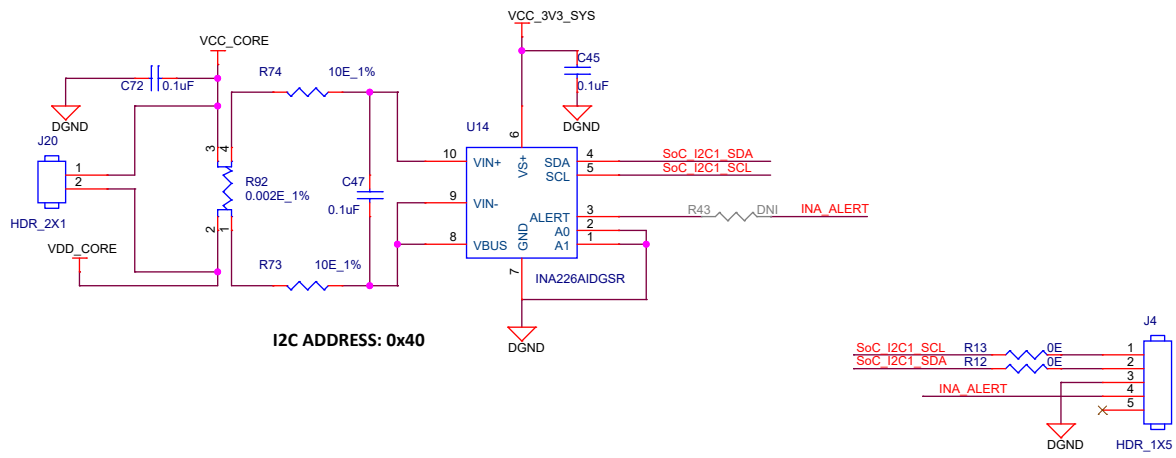
1. OSPI
2. MMC1 - SD CARD
3. MMC0 - eMMC
4. CPSW Ethernet Slave
5. USB Host
6. USB Device
7. UART
8. Ethernet

Off Page Connections

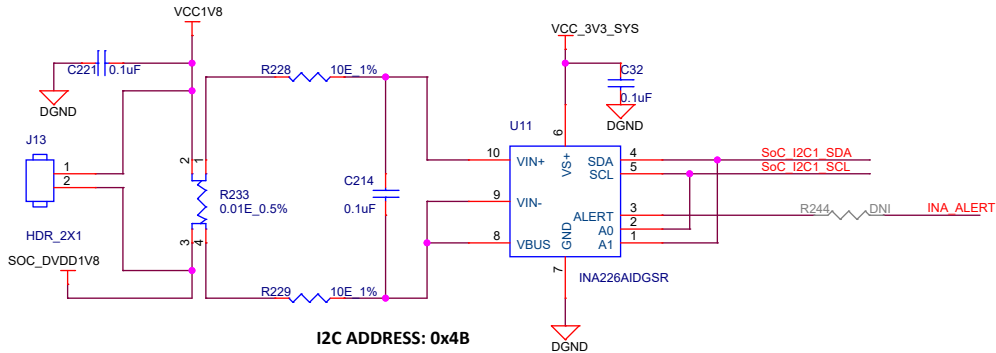


CURRENT MONITORING DEVICES

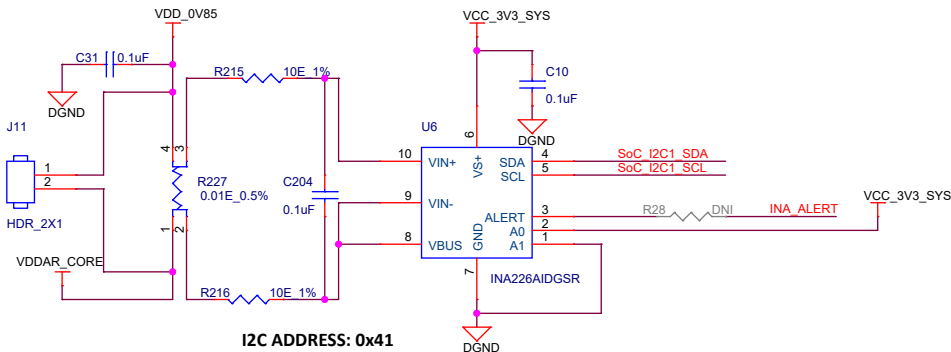
VDD_CORE



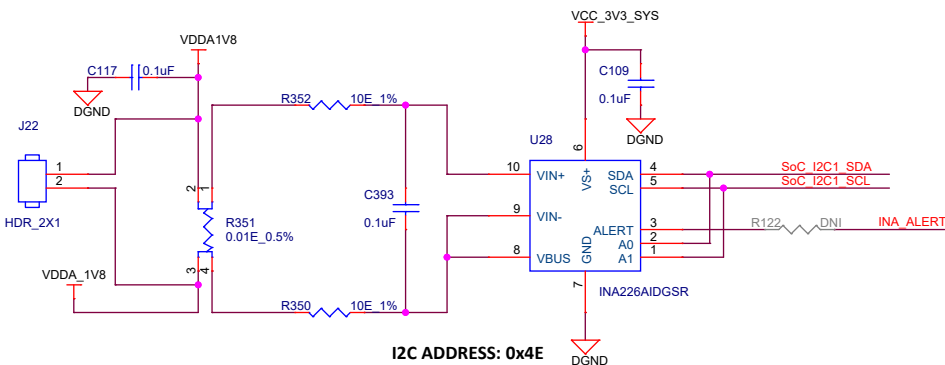
SoC_DVDD1V8



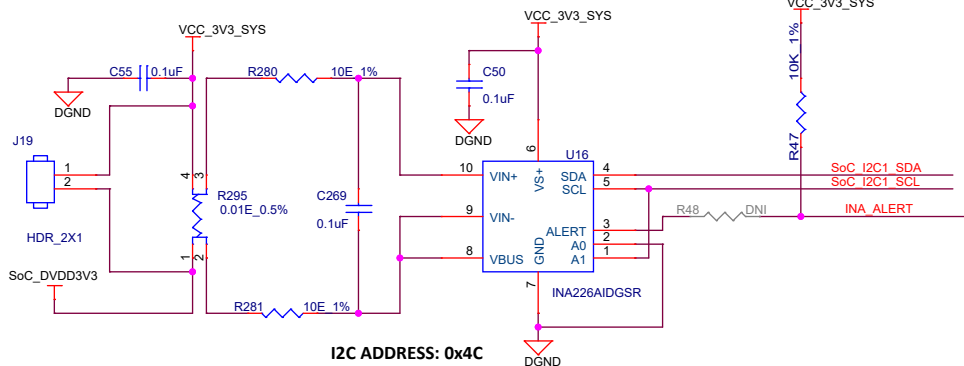
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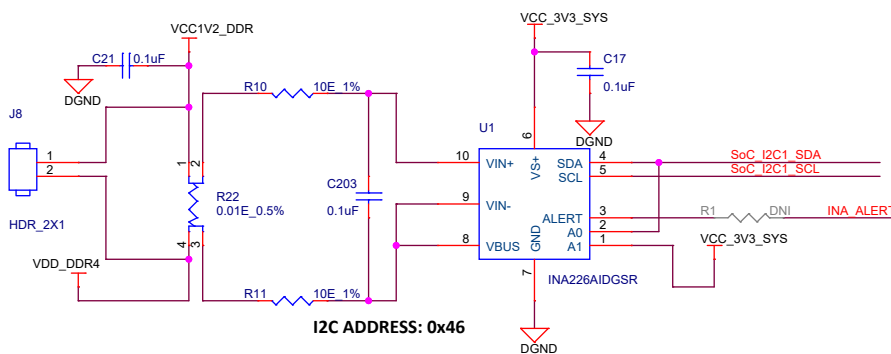
VDDA_1V8



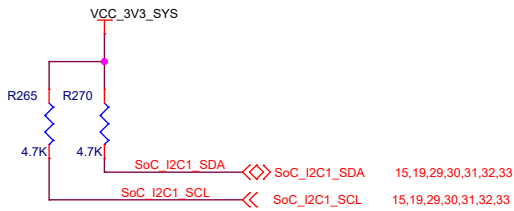
SoC_DVDD3V3



VDD_DDR4



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VDD_0V85	VDDAR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	4B
VDDA1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46



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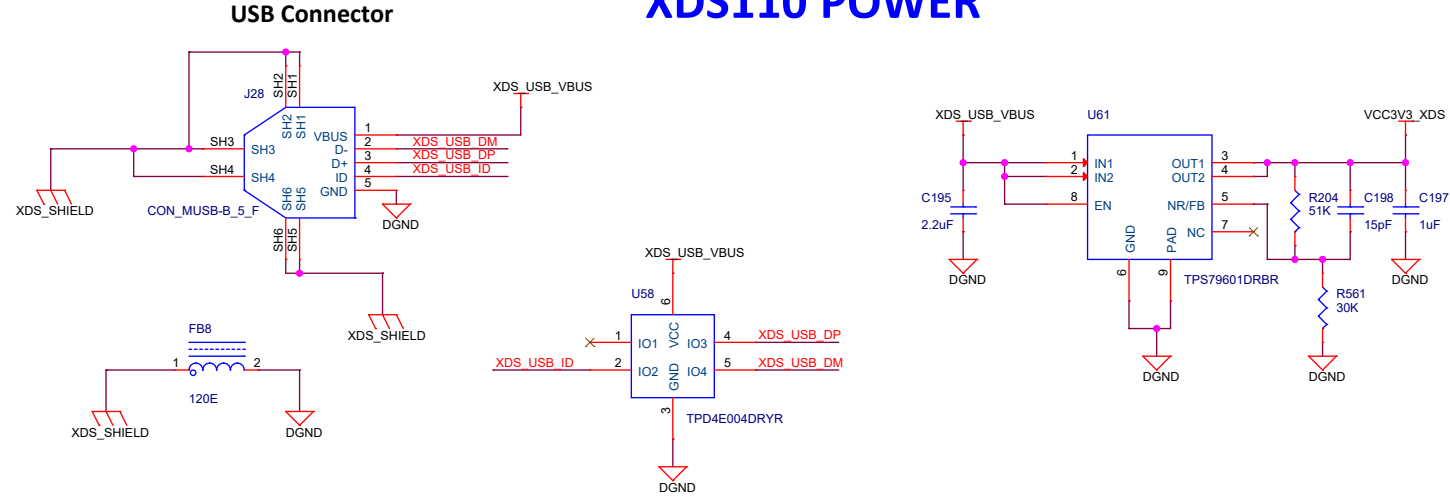


Title CURRENT MONITORING DEVICES

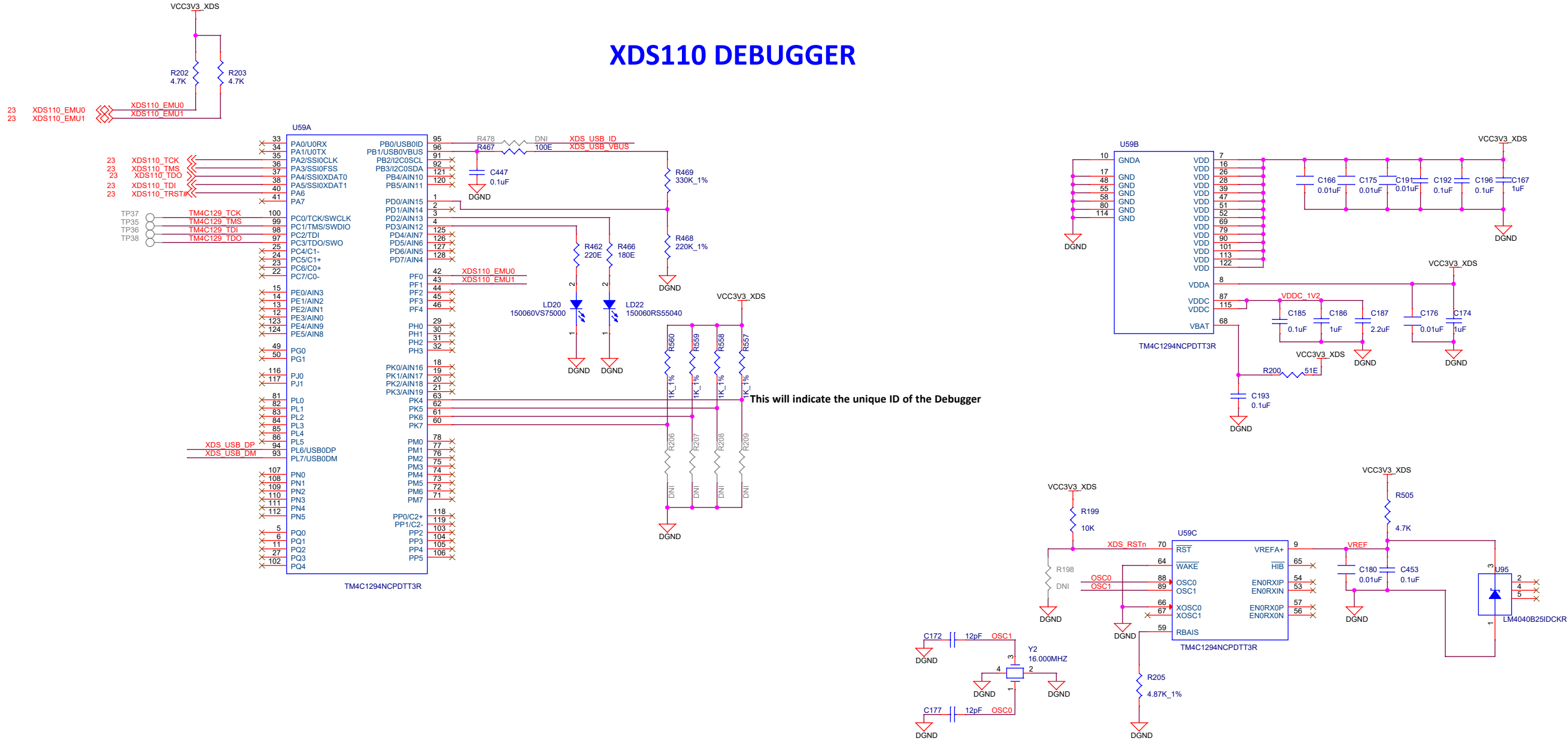
Size Variant Name = PROC101D(004) TMDs64EVM

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XDS110 POWER



XDS110 DEBUGGER



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Title XDS110 DEBUGGER

Size
C Variant Name = PROC101D(004) TMDs64EVM

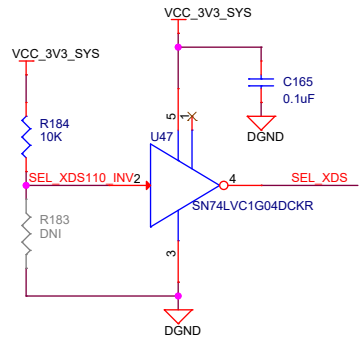
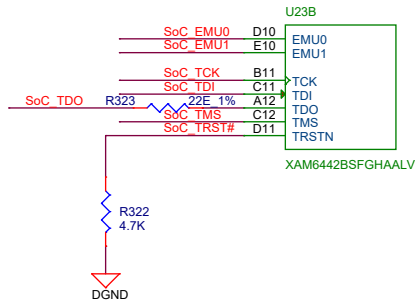
Rev
D

Date: Monday, November 27, 2023

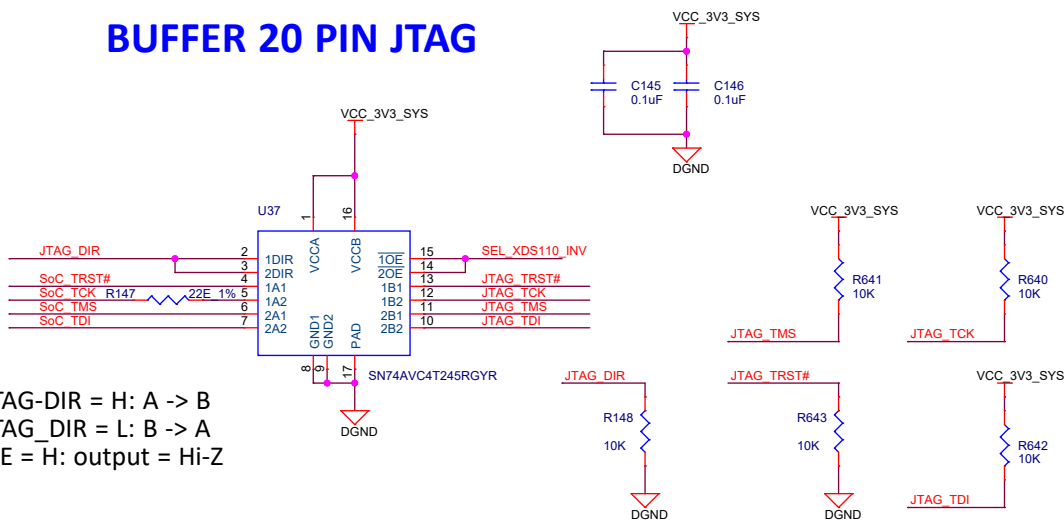
Sheet 22 of 40

JTAG BUFFER

JTAG SoC SECTION

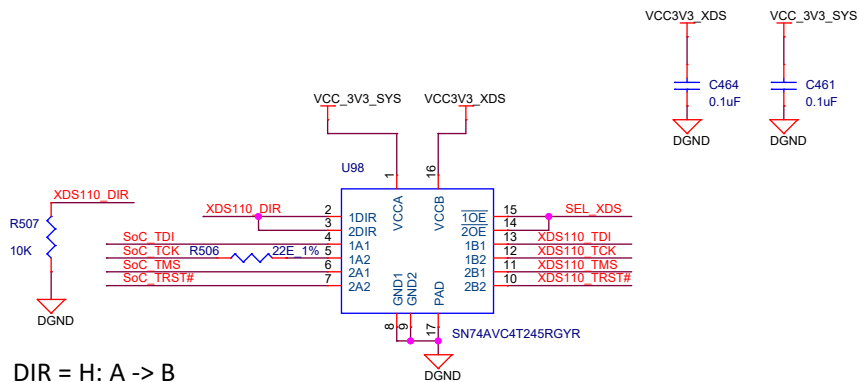


BUFFER 20 PIN JTAG



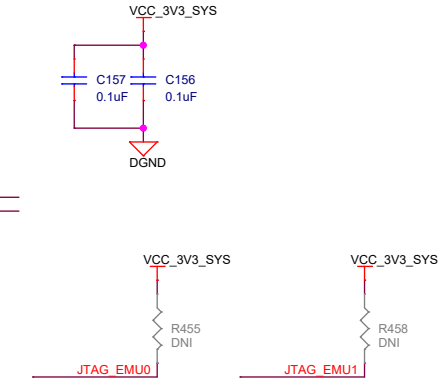
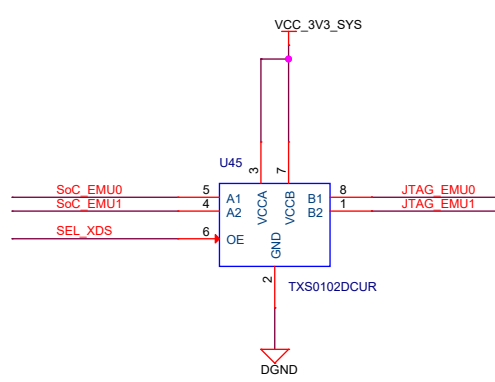
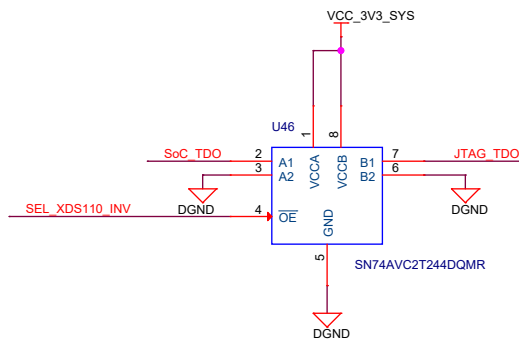
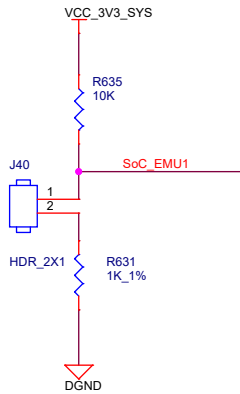
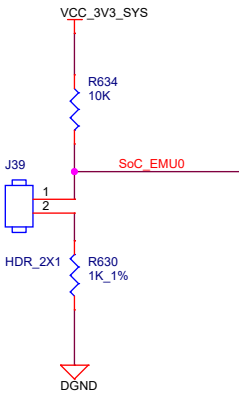
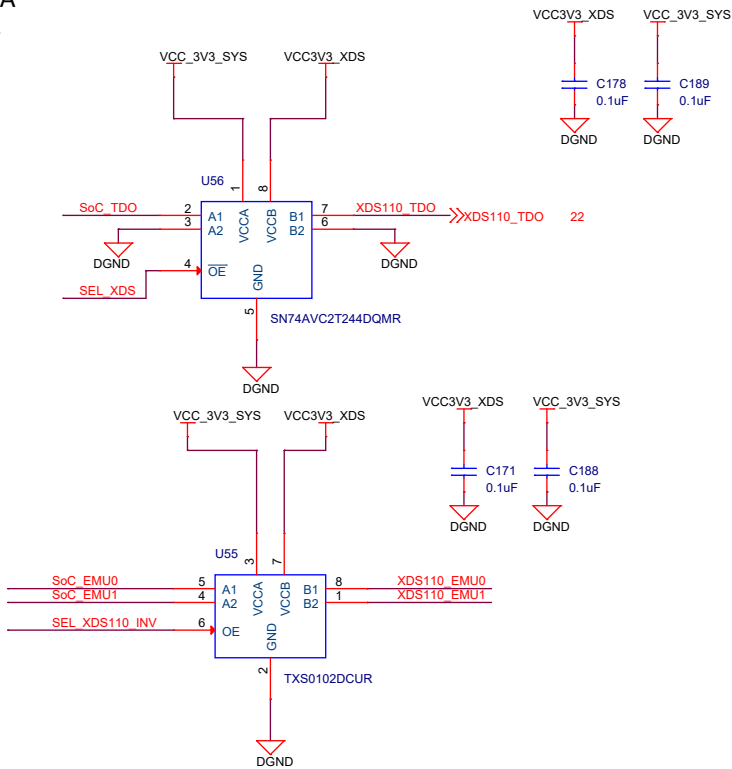
JTAG-DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = H: output = Hi-Z

BUFFER XDS110



XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z

Placement of Buffers U37, U46, U56 and U98 to be changed to reduce Stub length of the JTAG signals. These buffers need to be placed closer to the cTI-20pin connector -J25



Off Page Connections

24	SEL_XDS110_INV	SEL_XDS110_INV
24	JTAG_EMU0	JTAG_EMU0
24	JTAG_EMU1	JTAG_EMU1
22	XDS110_TDI	XDS110_TDI
22	XDS110_TCK	XDS110_TCK
22	XDS110_TMS	XDS110_TMS
22	XDS110_TRST#	XDS110_TRST#
24	JTAG_TDI	JTAG_TDI
24	JTAG_TCK	JTAG_TCK
24	JTAG_TMS	JTAG_TMS
24	JTAG_TRST#	JTAG_TRST#
24	JTAG_TDO	JTAG_TDO
24	XDS110_EMU0	XDS110_EMU0
22	XDS110_EMU1	XDS110_EMU1

From XDS1100 Debugger

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Title JTAG BUFFER

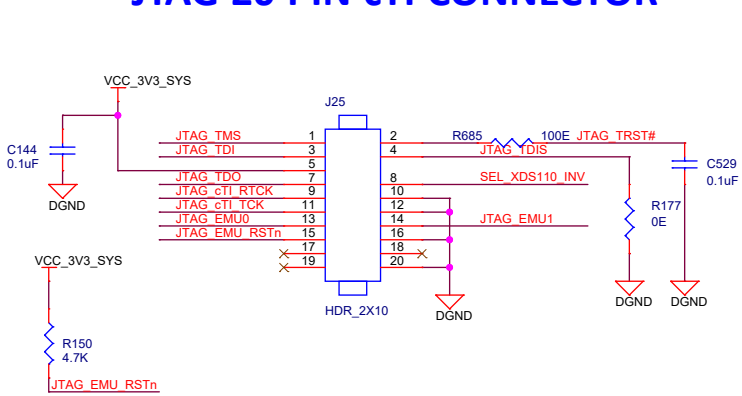
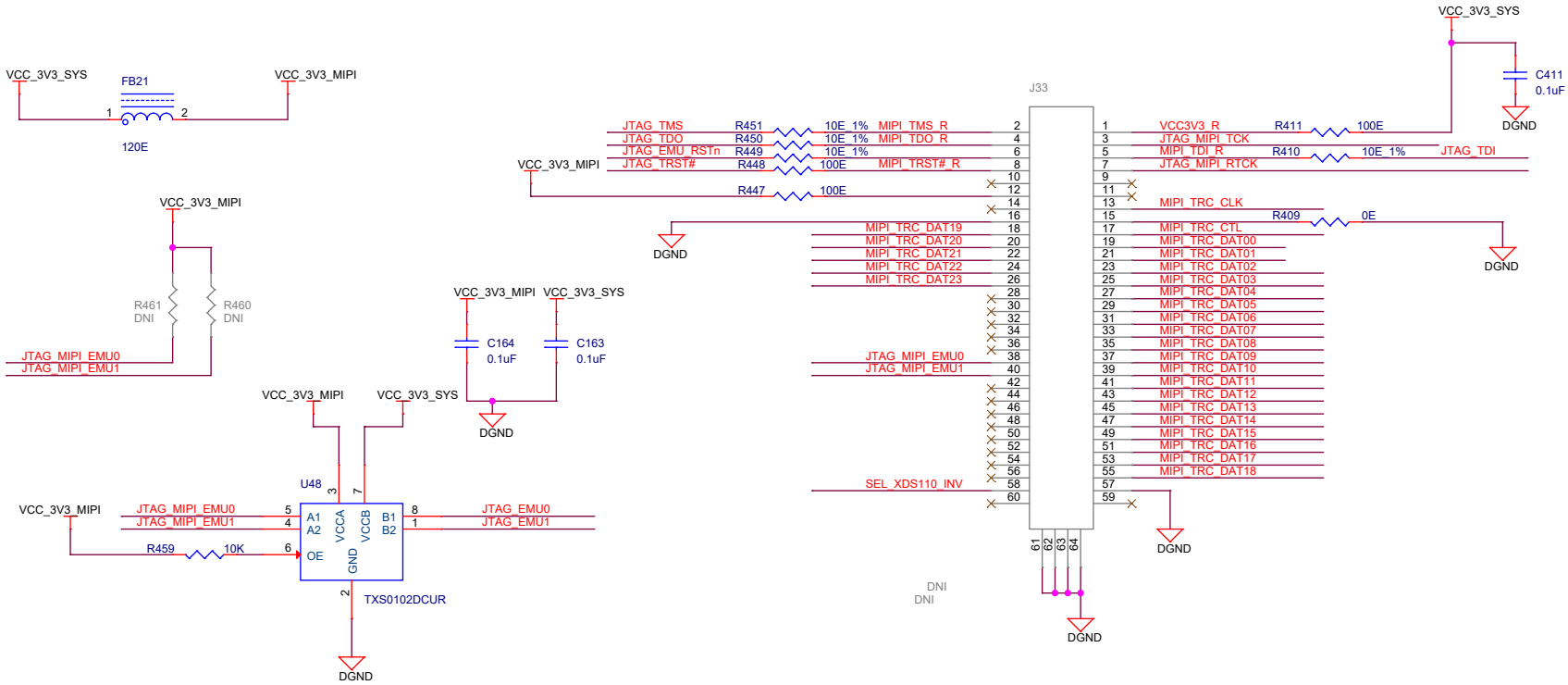
Size Variant Name = PROC101D(004) TMDs64EVM

Date: Monday, November 27, 2023

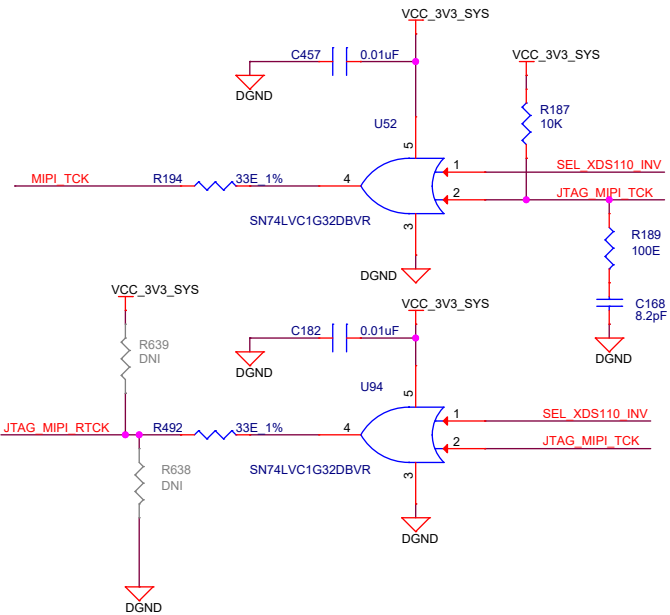
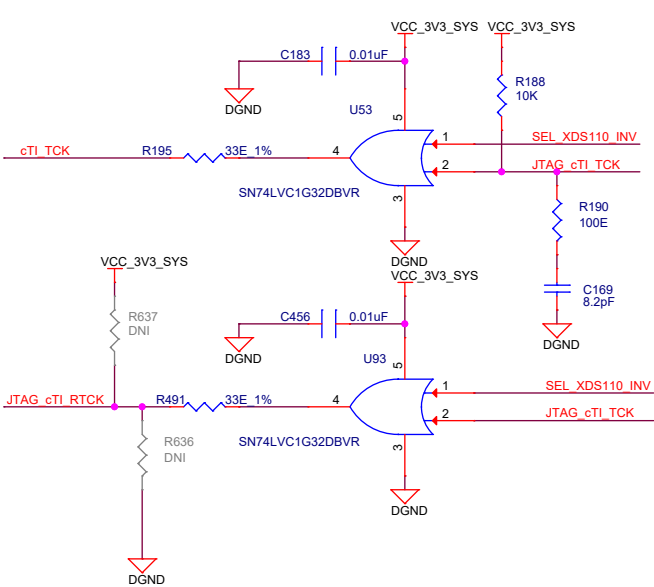
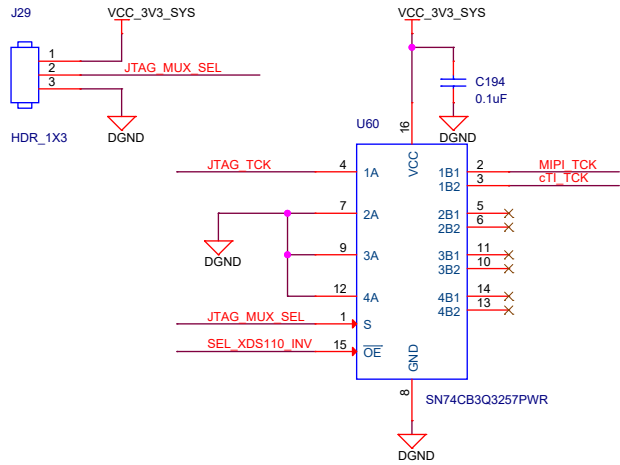
Sheet 23 of 40

MIPI 60 PIN CONNECTOR

JTAG 20 PIN cTI CONNECTOR

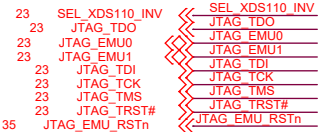


JTAG CLOCK BUFFER

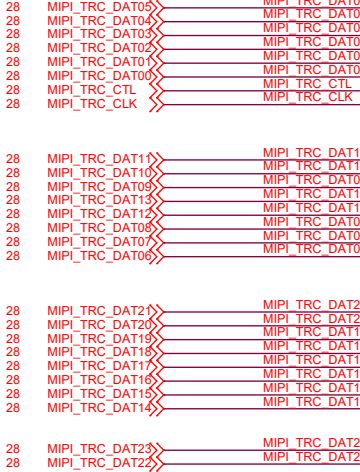


Off Page Connections

From JTAG Buffer



From SoC GPMC



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Title MIPI 60 PIN CONNECTOR

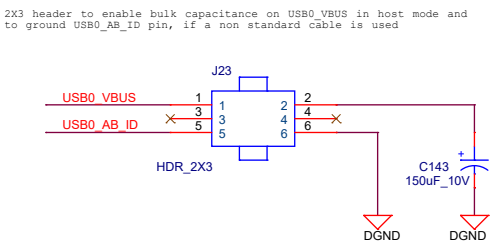
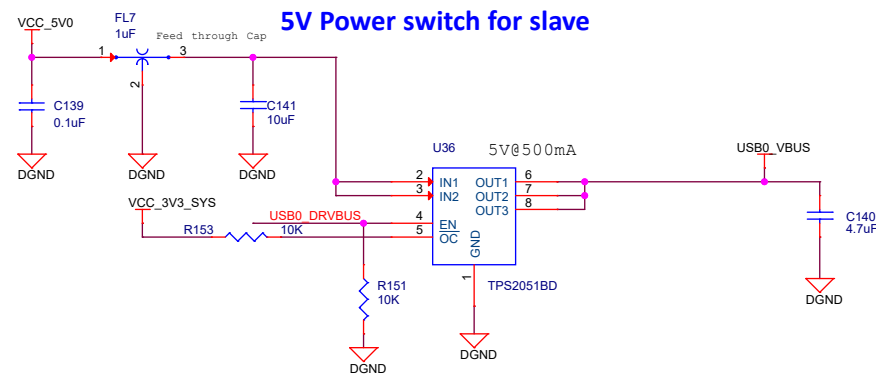
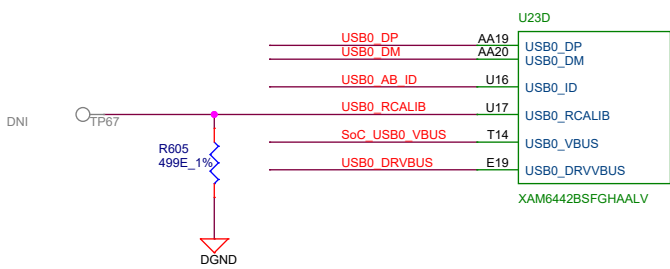
Size Variant Name = PROC101D(004) TMDSS64EVM

Date: Monday, November 27, 2023

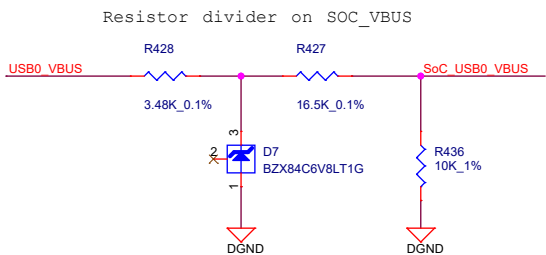
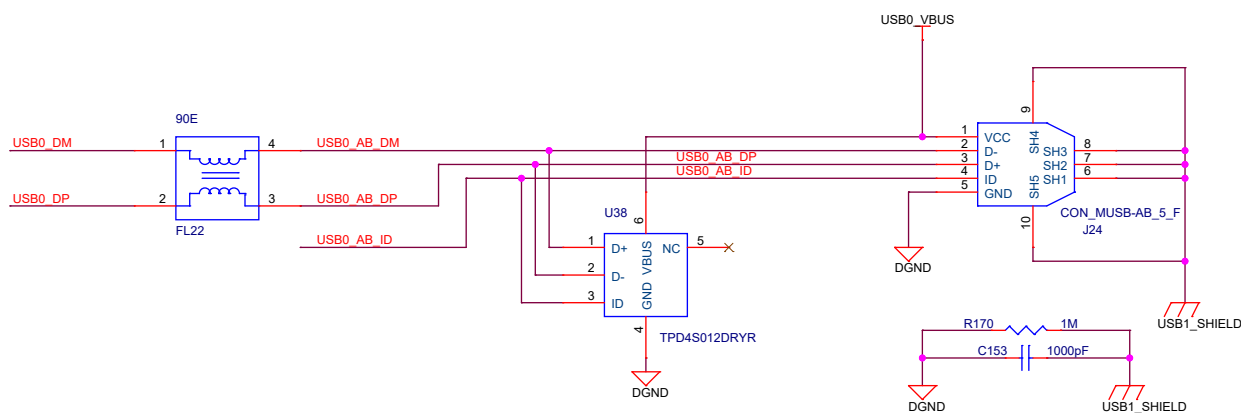
Rev D

Sheet 24 of 40

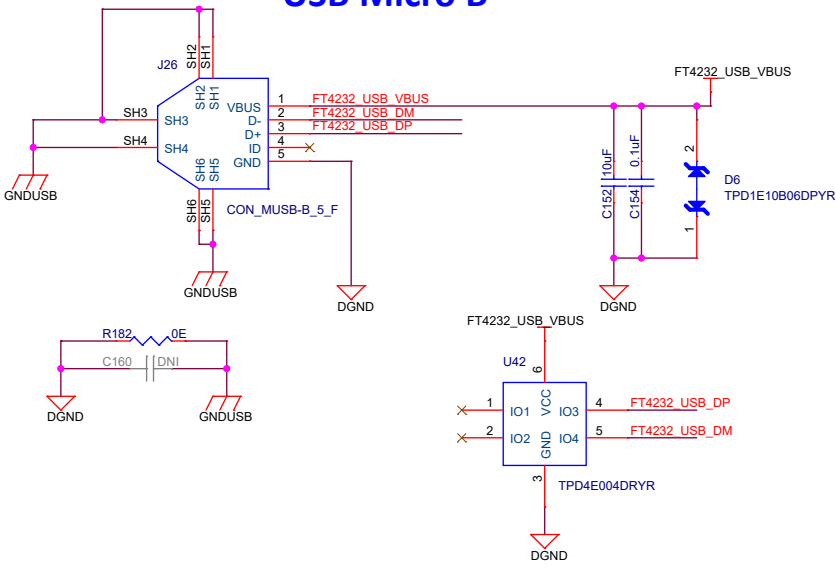
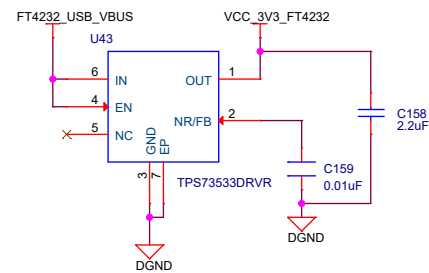
USB 2.0 INTERFACE



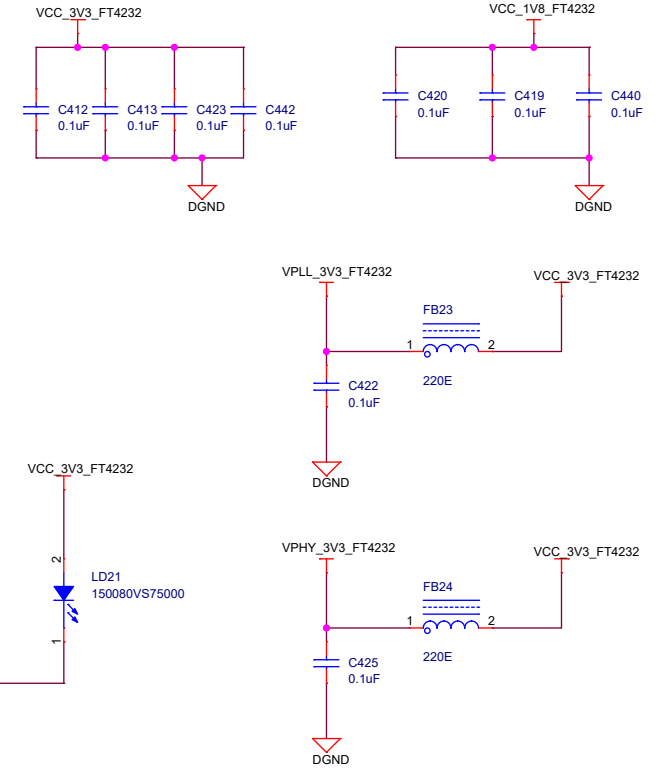
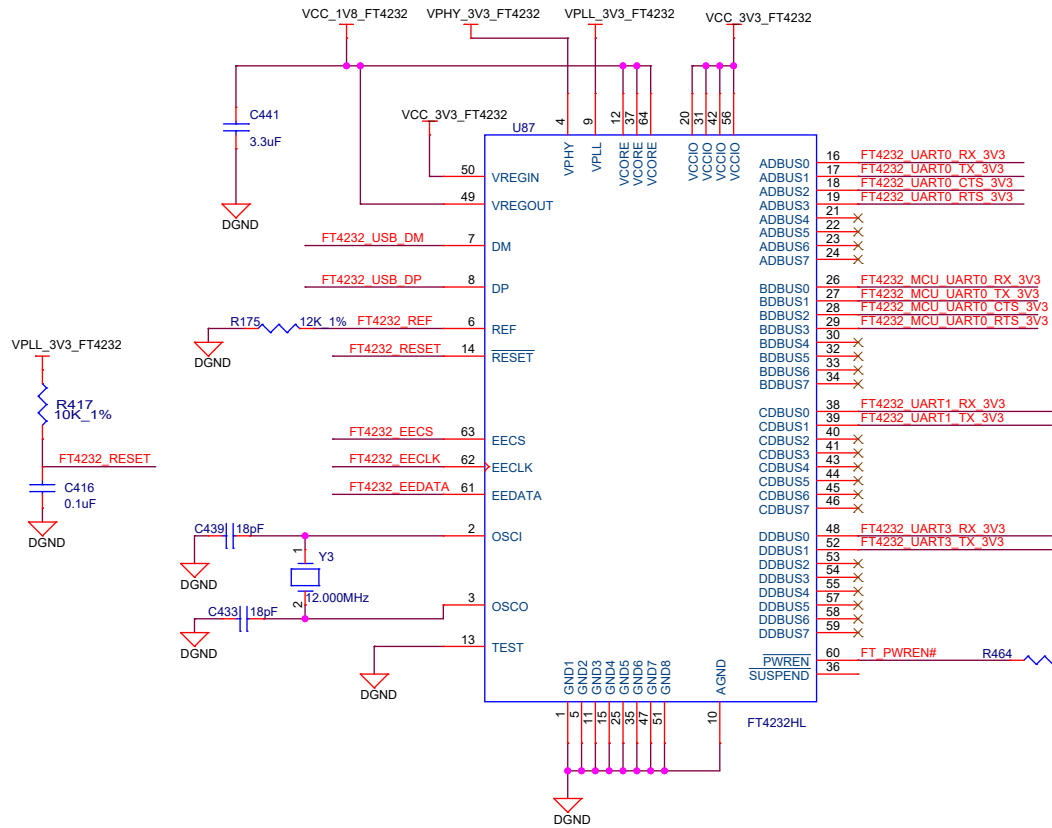
Micro USB 2.0 AB Connector



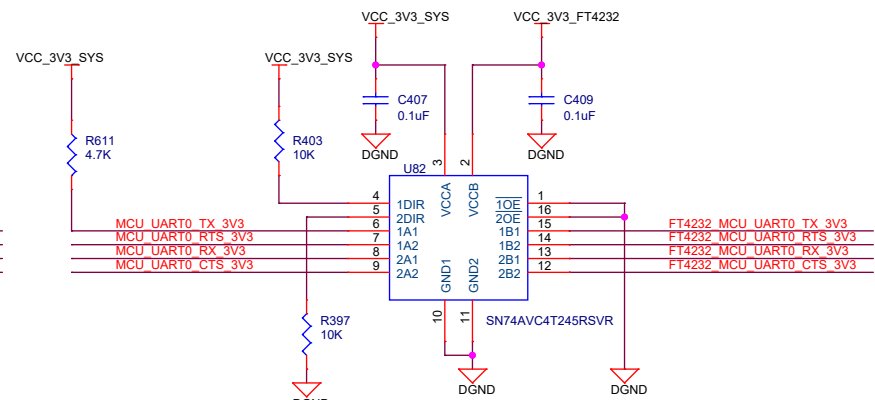
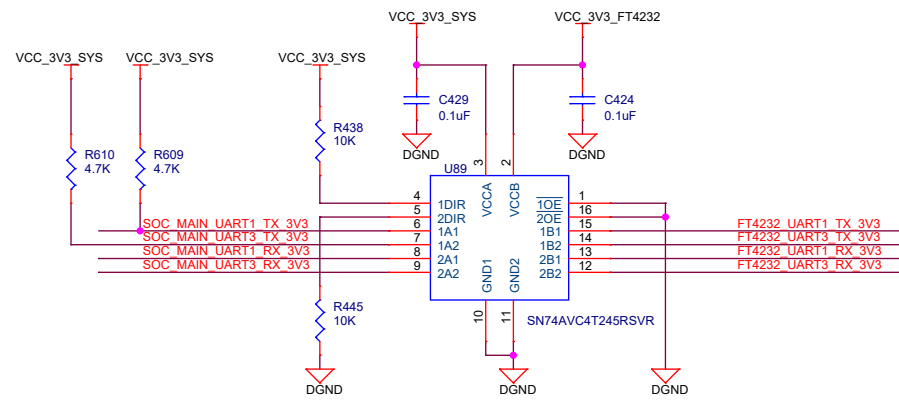
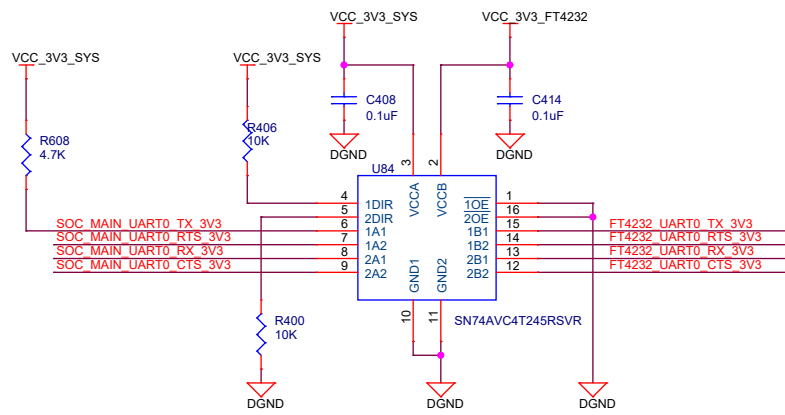
USB Micro B

**FT4232: 5V to 3.3V@500mA LDO**

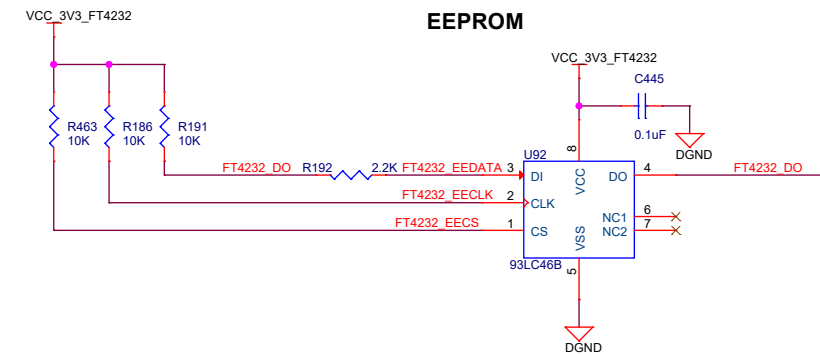
FT4232 UART



FT4232 LEVEL TRANSLATOR



EEPROM



Off Page Connections

SOC_MAIN_UART0_RX_3V3	29
SOC_MAIN_UART0_TX_3V3	29
SOC_MAIN_UART0_RTS_3V3	29
SOC_MAIN_UART0_CTS_3V3	29
MCU_UART0_RX_3V3	34
MCU_UART0_TX_3V3	34
MCU_UART0_RTS_3V3	34
MCU_UART0_CTS_3V3	34
SOC_MAIN_UART1_RX_3V3	29
SOC_MAIN_UART1_TX_3V3	29
SOC_MAIN_UART1_RTS_3V3	29
SOC_MAIN_UART1_CTS_3V3	29

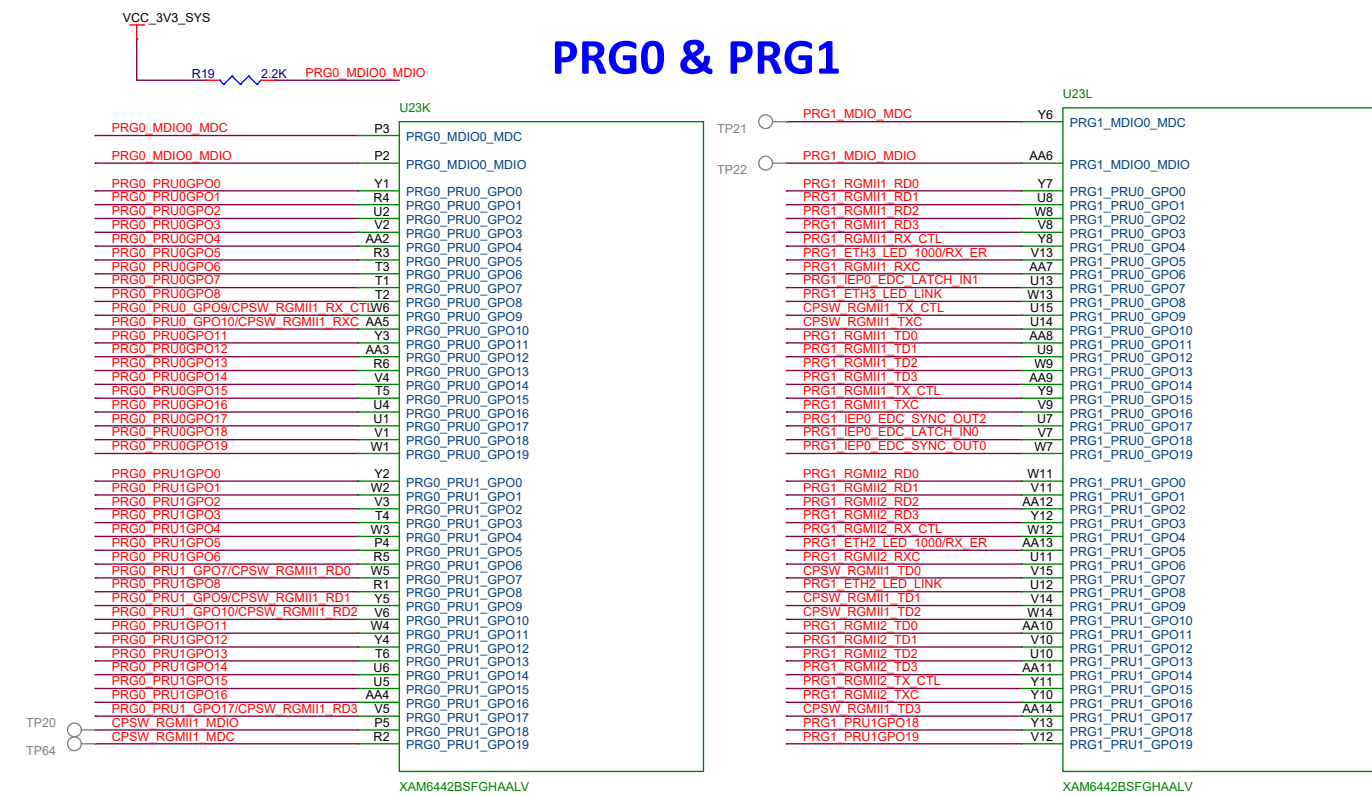
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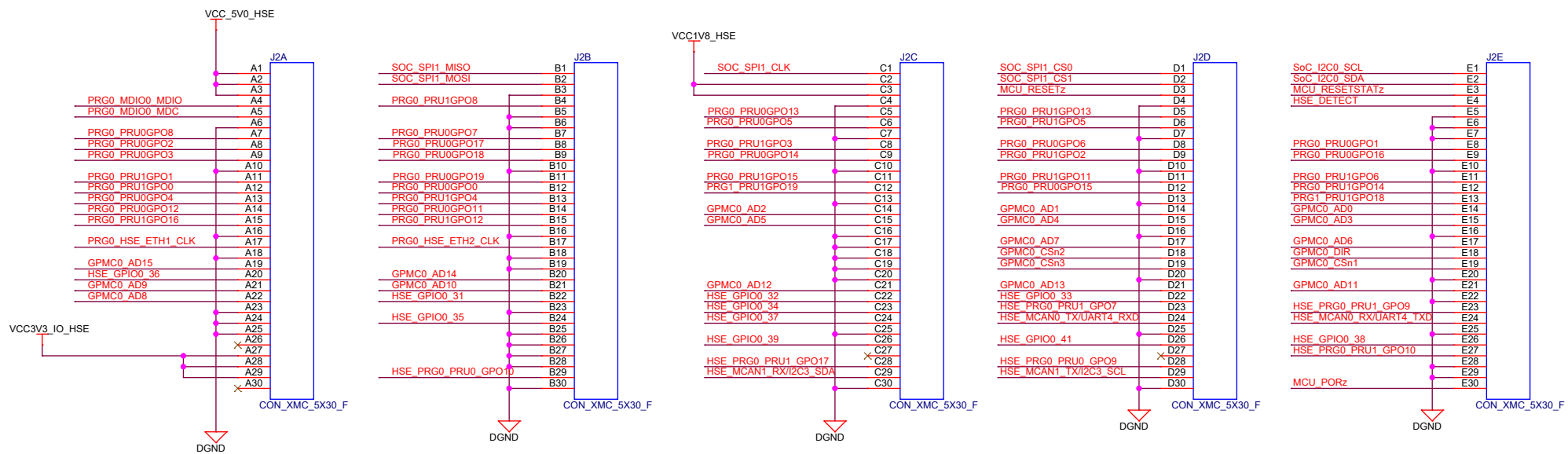
Title	FT4232 UART TO USB BRIDGE
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Size	Variant Name = PROC101D(004) TMSD64EVM	Rev
C		D
Date:	Monday, November 27, 2023	Sheet 26 of 40

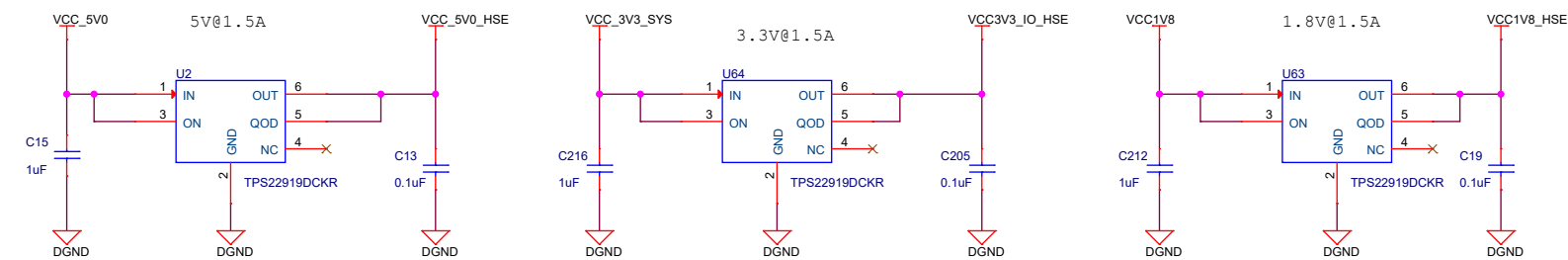
PRG0 & PRG1



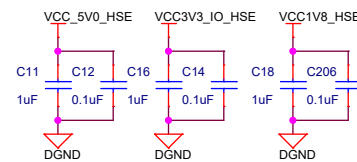
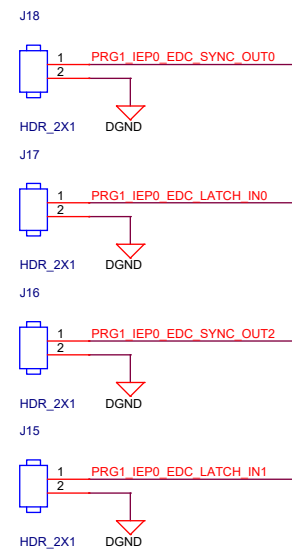
HIGH SPEED EXPANSION CONNECTOR



HSE CONNECTOR LOAD SWITCHES



SYNC TP



Off Page Connections

To Presence Detect Buffer	15	HSE_DETECT	<<	HSE_DETECT
From Processor GPMC	28	GPMC0_CSn1	>>	GPMC0_CSn2
	28	GPMC0_CSn2	>>	GPMC0_CSn3
	28	GPMC0_CSn3	>>	GPMC0_DIR
	28	GPMC0_DIR	>>	
From FSI mux	28	GPMC0_AD8	>>	GPMC0_AD8
	28	GPMC0_AD9	>>	GPMC0_AD9
	28	GPMC0_AD10	>>	GPMC0_AD10
	28	GPMC0_AD11	>>	GPMC0_AD14
	28	GPMC0_AD14	>>	GPMC0_AD15
	28	GPMC0_AD15	>>	HSE_GPI00_36
	28	HSE_GPI00_36	>>	
From Processor GPMC resistor muxed with MIPI	28	GPMC0_AD0	>>	GPMC0_AD0
	28	GPMC0_AD1	>>	GPMC0_AD1
	28	GPMC0_AD2	>>	GPMC0_AD2
	28	GPMC0_AD3	>>	GPMC0_AD3
	28	GPMC0_AD4	>>	GPMC0_AD4
	28	GPMC0_AD5	>>	GPMC0_AD5
	28	GPMC0_AD6	>>	GPMC0_AD6
	28	GPMC0_AD7	>>	GPMC0_AD7
	28	GPMC0_AD7	>>	
	28	GPMC0_AD11	>>	GPMC0_AD11
	28	GPMC0_AD12	>>	GPMC0_AD12
	28	GPMC0_AD13	>>	GPMC0_AD13
	28	GPMC0_AD13	>>	
	28	HSE_GPI00_31	>>	HSE_GPI00_31
	28	HSE_GPI00_32	>>	HSE_GPI00_32
	28	HSE_GPI00_33	>>	HSE_GPI00_33
	28	HSE_GPI00_34	>>	HSE_GPI00_34
	28	HSE_GPI00_35	>>	HSE_GPI00_35
	28	HSE_GPI00_36	>>	
	28	HSE_GPI00_37	>>	HSE_GPI00_37
	28	HSE_GPI00_38	>>	HSE_GPI00_38
	28	HSE_GPI00_39	>>	
	28	HSE_GPI00_40	>>	HSE_GPI00_39
	28	HSE_GPI00_41	>>	HSE_GPI00_41
	28	HSE_GPI00_42	>>	
From Processor	34	MCU_PORz	>>	MCU_PORz
	34,35	MCU_RESEtZ	>>	MCU_RESEtZ
	34	MCU_RESEtStAtZ	>>	MCU_RESEtStAtZ
	29	HSE_MCAN0_RX/UART4_TXD	>>	HSE_MCAN0_RX/UART4_TXD
	29	HSE_MCAN0_TX/UART4_RXD	>>	HSE_MCAN0_TX/UART4_RXD
	29	HSE_MCAN1_RX/I2C3_SDA	>>	HSE_MCAN1_RX/I2C3_SDA
	29	HSE_MCAN1_TX/I2C3_SCL	>>	HSE_MCAN1_TX/I2C3_SCL
	29	SOC_SPI1_CLK	>>	SOC_SPI1_CLK
	29	SOC_SPI1_MOSI	>>	SOC_SPI1_MOSI
	29	SOC_SPI1_MISO	>>	SOC_SPI1_MISO
	29	SOC_SPI1_CS0	>>	SOC_SPI1_CS0
	29	SOC_SPI1_CS1	>>	SOC_SPI1_CS1
	15,29,33	SoC_I2C0_SCL	>>	SoC_I2C0_SCL
	15,29,33	SoC_I2C0_SDA	>>	SoC_I2C0_SDA
From clock Buffer	31	PRG0_HSE_ETH1_CLK	>>	PRG0_HSE_ETH1_CLK
	31	PRG0_HSE_ETH2_CLK	>>	PRG0_HSE_ETH2_CLK
To and from ICSSG1 RGMII 2 Ethernet PHY	17	PRG1_RGMII2_RD0	>>	PRG1_RGMII2_RD0
	17	PRG1_RGMII2_RD1	>>	PRG1_RGMII2_RD1
	17	PRG1_RGMII2_RD2	>>	PRG1_RGMII2_RD2
	17	PRG1_RGMII2_RD3	>>	PRG1_RGMII2_RD3
	17	PRG1_RGMII2_RXC	>>	PRG1_RGMII2_RXC
	17	PRG1_RGMII2_RX_CTL	>>	PRG1_RGMII2_RX_CTL
	17	PRG1_ETH2_LED_1000/RX_ER	>>	PRG1_ETH2_LED_1000/RX_ER
	17	PRG1_RGMII2_TD0	>>	PRG1_RGMII2_TD0
	17	PRG1_RGMII2_TD1	>>	PRG1_RGMII2_TD1
	17	PRG1_RGMII2_TD2	>>	PRG1_RGMII2_TD2
	17	PRG1_RGMII2_TD3	>>	PRG1_RGMII2_TD3
	17	PRG1_RGMII2_TXC	>>	PRG1_RGMII2_TXC
	17	PRG1_RGMII2_TX_CTL	>>	PRG1_RGMII2_TX_CTL
	17,18	PRG1_MDIO_MDIO	>>	PRG1_MDIO_MDIO
	17,18	PRG1_MDIO_MDC	>>	PRG1_MDIO_MDC
	18	PRG1_ETH3_LED_LINK	>>	PRG1_ETH3_LED_LINK
To and from ICSSG2 RGMII 1 Ethernet PHY	17	PRG1_ETH2_LED_LINK	>>	PRG1_ETH2_LED_LINK
	18	PRG1_RGMII1_RD0	>>	PRG1_RGMII1_RD0
	18	PRG1_RGMII1_RD1	>>	PRG1_RGMII1_RD1
	18	PRG1_RGMII1_RD2	>>	PRG1_RGMII1_RD2
	18	PRG1_RGMII1_RD3	>>	PRG1_RGMII1_RD3
	18	PRG1_RGMII1_RXC	>>	PRG1_RGMII1_RXC
	18	PRG1_RGMII1_RX_CTL	>>	PRG1_RGMII1_RX_CTL
	18	PRG1_ETH3_LED_1000/RX_ER	>>	PRG1_ETH3_LED_1000/RX_ER
	18	PRG1_RGMII1_TD0	>>	PRG1_RGMII1_TD0
	18	PRG1_RGMII1_TD1	>>	PRG1_RGMII1_TD1
	18	PRG1_RGMII1_TD2	>>	PRG1_RGMII1_TD2
	18	PRG1_RGMII1_TD3	>>	PRG1_RGMII1_TD3
	18	PRG1_RGMII1_TXC	>>	PRG1_RGMII1_TXC
	18	PRG1_RGMII1_TX_CTL	>>	PRG1_RGMII1_TX_CTL
From MUX To HSE	16	HSE_PRG0_PRU1_GP07	>>	HSE_PRG0_PRU1_GP07
	16	HSE_PRG0_PRU1_GP09	>>	HSE_PRG0_PRU1_GP09
	16	HSE_PRG0_PRU1_GP010	>>	HSE_PRG0_PRU1_GP010
	16	HSE_PRG0_PRU1_GP017	>>	HSE_PRG0_PRU1_GP017
	16	HSE_PRG0_PRU0_GP09	>>	HSE_PRG0_PRU0_GP09
	16	HSE_PRG0_PRU0_GP010	>>	HSE_PRG0_PRU0_GP010
	16,17	CPSW_RGMII1_MDIO	>>	CPSW_RGMII1_MDIO
	16,17	CPSW_RGMII1_MDC	>>	CPSW_RGMII1_MDC
To MUX From SoC	16	PRG0_PRU1_GP07/CPSW_RGMII1_RD0	>>	PRG0_PRU1_GP07/CPSW_RGMII1_RD0
	16	PRG0_PRU1_GP09/CPSW_RGMII1_RD1	>>	PRG0_PRU1_GP09/CPSW_RGMII1_RD1
	16	PRG0_PRU1_GP010/CPSW_RGMII1_RD2	>>	PRG0_PRU1_GP010/CPSW_RGMII1_RD2
	16	PRG0_PRU1_GP017/CPSW_RGMII1_RD3	>>	PRG0_PRU1_GP017/CPSW_RGMII1_RD3
	16	PRG0_PRU0_GP09/CPSW_RGMII1_RX_CTL	>>	PRG0_PRU0_GP09/CPSW_RGMII1_RX_CTL
	16	PRG0_PRU0_GP010/CPSW_RGMII1_TXC	>>	PRG0_PRU0_GP010/CPSW_RGMII1_TXC

GPMC

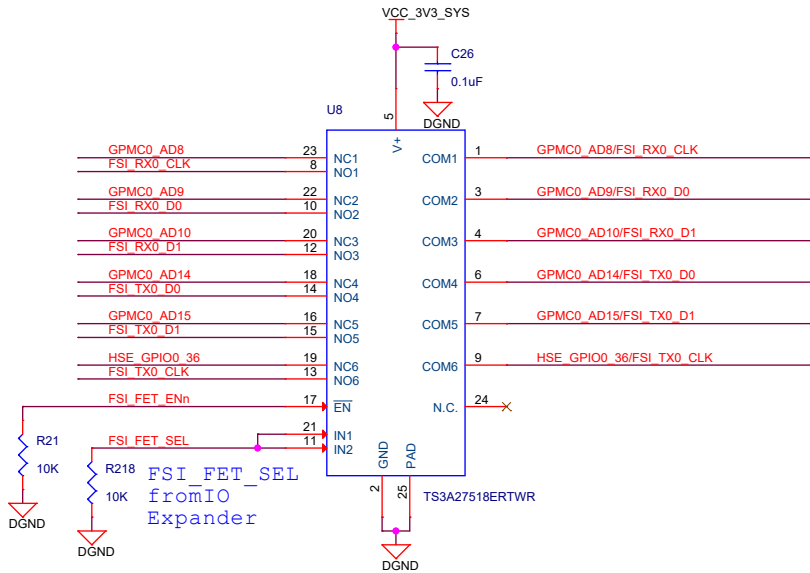
To Boot Mode Buffer ,
HSE & MIPI Conn

20 BOOTMODE0
20 BOOTMODE1
20 BOOTMODE2
20 BOOTMODE3
20 BOOTMODE4
20 BOOTMODE5
20 BOOTMODE6
20 BOOTMODE7
20 BOOTMODE8
20 BOOTMODE9
20 BOOTMODE10
20 BOOTMODE11
20 BOOTMODE12
20 BOOTMODE13
20 BOOTMODE14
20 BOOTMODE15

GPMC0_CLK R17 GPMC0_CLK
BOOTMODE0 T20 GPMC0_AD0
BOOTMODE1 U21 GPMC0_AD1
BOOTMODE2 T18 GPMC0_AD2
BOOTMODE3 U20 GPMC0_AD3
BOOTMODE4 U18 GPMC0_AD4
BOOTMODE5 U19 GPMC0_AD5
BOOTMODE6 V20 GPMC0_AD6
BOOTMODE7 V21 GPMC0_AD7
BOOTMODE8 T17 GPMC0_AD8
BOOTMODE9 T16 GPMC0_AD9
BOOTMODE10 W20 GPMC0_AD10
BOOTMODE11 W21 GPMC0_AD11
BOOTMODE12 W18 GPMC0_AD12
BOOTMODE13 Y21 GPMC0_AD13
BOOTMODE14 Y21 GPMC0_AD14
BOOTMODE15 Y20 GPMC0_AD15
GPMC0_CSn0 R19 GPMC0_CSn0
GPMC0_CSn1 R20 GPMC0_CSn1
GPMC0_CSn2 P19 GPMC0_CSn2
GPMC0_CSn3 R21 GPMC0_CSn3
GPMC0_ADVn_ALE P16 GPMC0_ADVN_ALE
GPMC0_BE0n_CLE P17 GPMC0_BE0N_CLE
GPMC0_BE1n T19 GPMC0_BE1N
GPMC0_DIR N17 GPMC0_DIR
GPMC0_WAIT0 W19 GPMC0_WAIT0
GPMC0_WAIT1 Y18 GPMC0_WAIT1
GPMC0_WPh N16 GPMC0_WPN
GPMC0_OEn_REn R18 GPMC0_OEN_REN
GPMC0_WEn T21 GPMC0_WEN

XAM6442BSFGHAALV

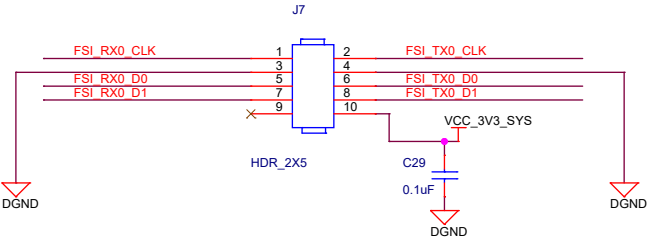
GPMC TO FSI & HSE CONNECTOR



TS3A27518ERTWR Truth Table

EN#	IN1	IN2	NC1/2/3 TO COM1/2/3 & COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM14/5/6 & COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3 & COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM14/5/6 & COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

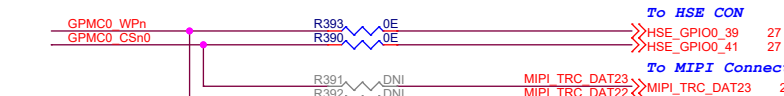
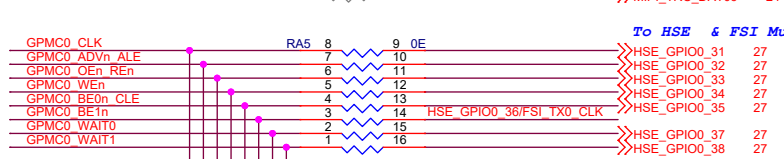
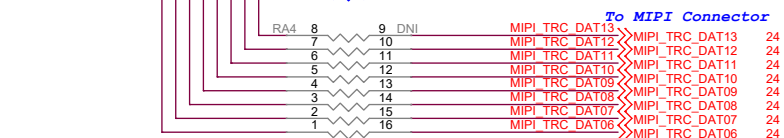
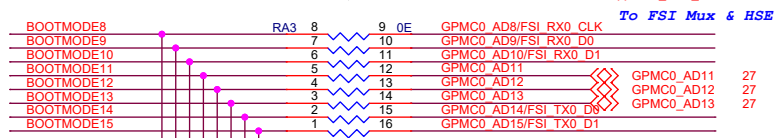
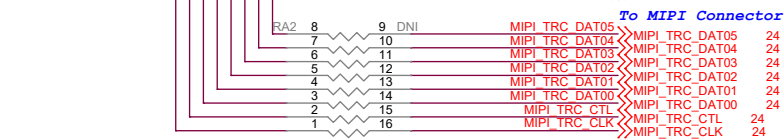
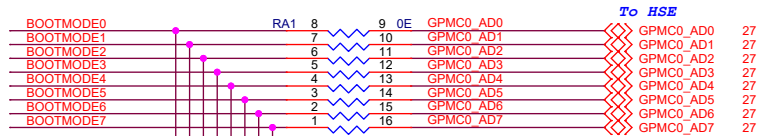
FSI CONNECTOR



0- Ohm Res MUX between HSE Connector and TRACE Functionality

-For HSE Connector RA1, RA3, RA5, R393 & R390 Should be installed and RA2, RA4, RA6, R391 & R392 Should be DNI'd.

-For TRACE RA2, RA4, RA6, R391 & R392 Should be Installed and RA1, RA3, RA5, R393 & R390 Should be DNI'd.



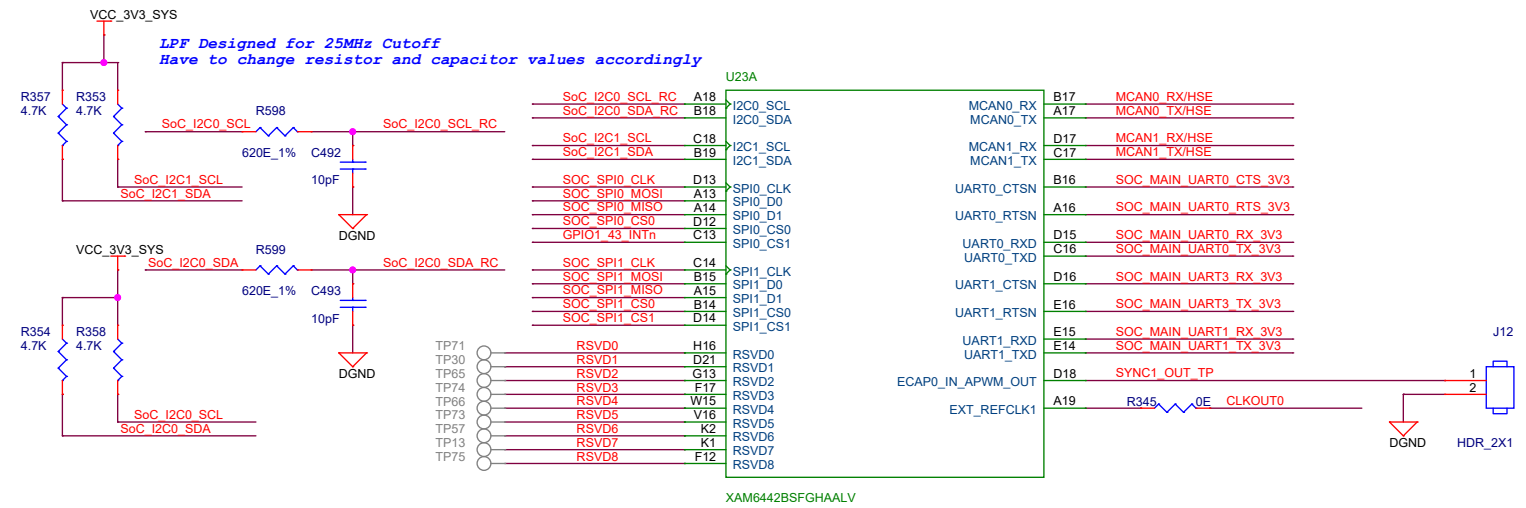
Off Page Connections

From IO Expander	33	FSI_FET_SEL	FSI_FET_SEL
To HSE Connector	27	GPMC0_CSn1	GPMC0_CSn1
	27	GPMC0_CSn2	GPMC0_CSn2
	27	GPMC0_CSn3	GPMC0_CSn3
	27	GPMC0_DIR	GPMC0_DIR
From FSI mux	27	GPMC0_AD8	GPMC0_AD8
To HSE Connector	27	GPMC0_AD9	GPMC0_AD9
	27	GPMC0_AD10	GPMC0_AD10
	27	GPMC0_AD14	GPMC0_AD14
	27	GPMC0_AD15	GPMC0_AD15
	27	HSE_GPIO0_36	HSE_GPIO0_36

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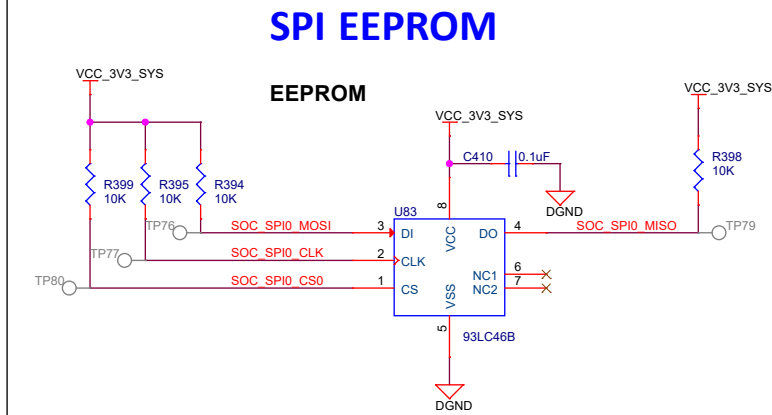
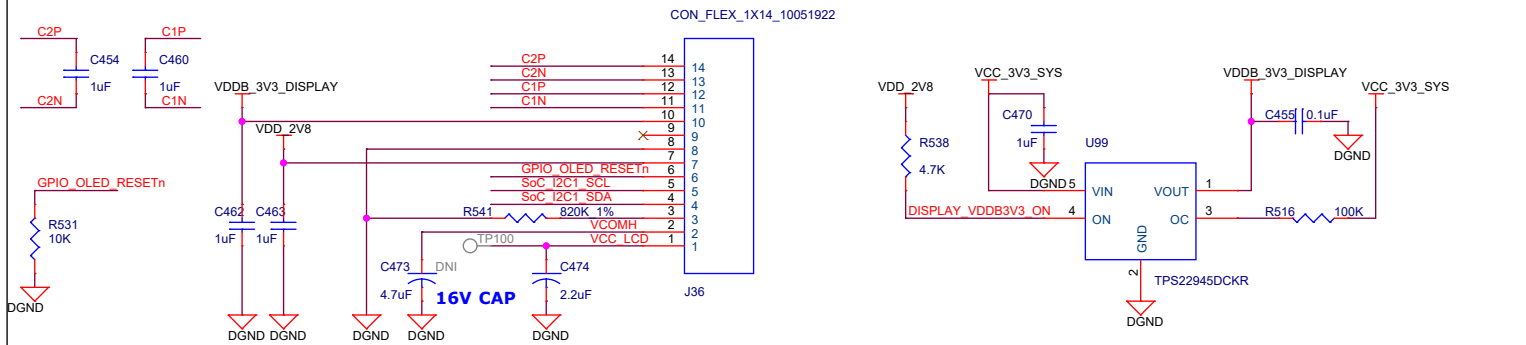


Title		GPMC	
Size			Rev
C	Variant Name = PROC101D(004) TMDs64EVM		D
Date:	Monday, November 27, 2023	Sheet	28 of 40



DISPLAY

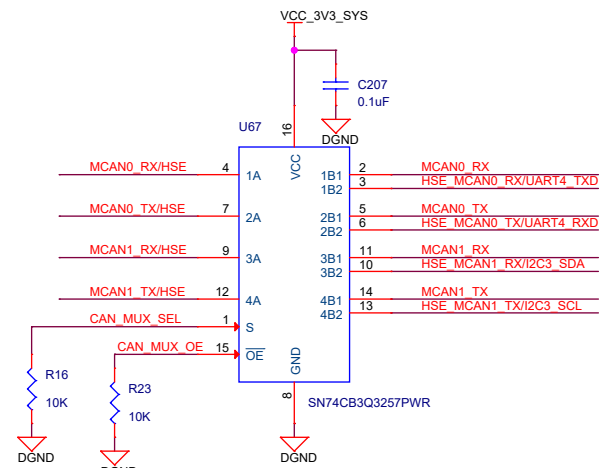
DISPLAY CONNECTOR



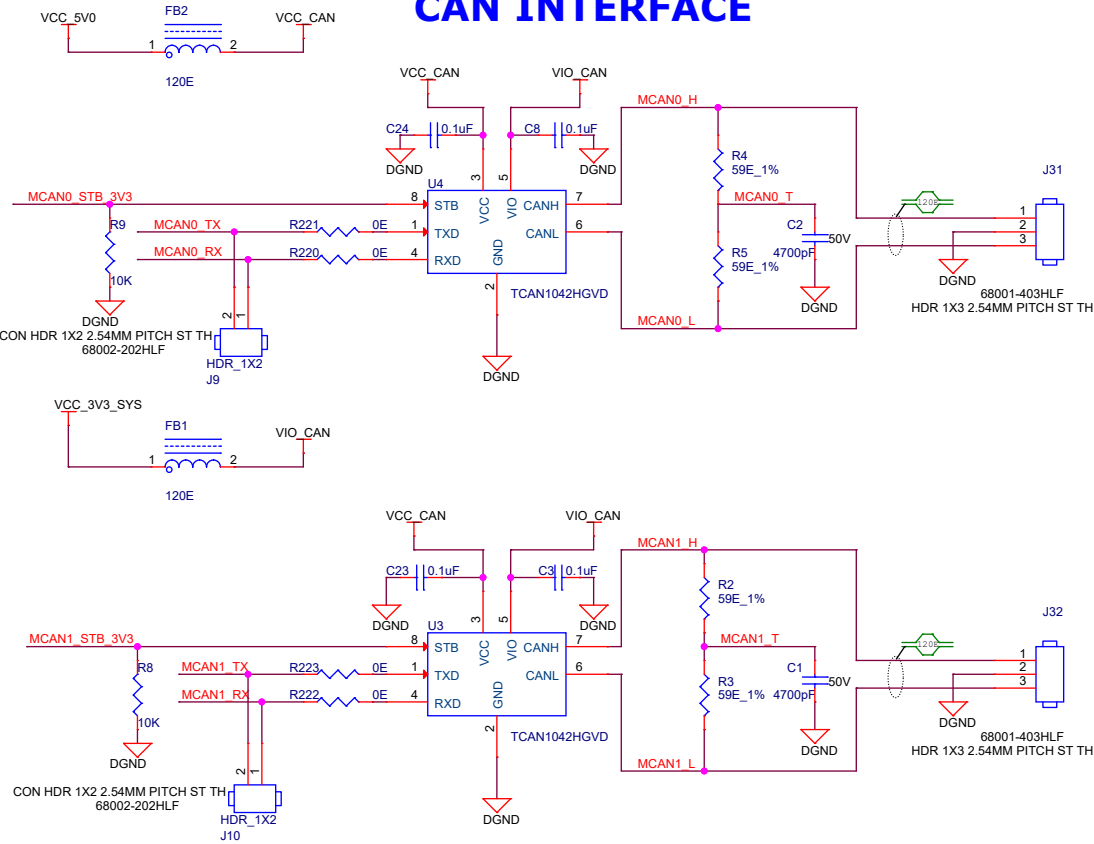
Off Page Connections

From Debounce Circuit	GPIO1_43_IN1n	GPIO1_43_IN1n	35
From IO Expander	GPIO_OLED_RESETh	GPIO_OLED_RESETh	33
From IO Expander	MCAN0_STB_3V3	MCAN0_STB_3V3	33
From IO Expander	MCAN1_STB_3V3	MCAN1_STB_3V3	33
From IO Expander	CAN_MUX_SEL	CAN_MUX_SEL	33
To HSE Connector	HSE_MCAN0_RX/UART4_TXD	HSE_MCAN0_RX/UART4_TXD	27
To HSE Connector	HSE_MCAN0_TX/UART4_RXD	HSE_MCAN0_TX/UART4_RXD	27
To HSE Connector	HSE_MCAN1_RX/I2C3_SDA	HSE_MCAN1_RX/I2C3_SDA	27
To HSE Connector	HSE_MCAN1_TX/I2C3_SCL	HSE_MCAN1_TX/I2C3_SCL	27
To HSE Connector	SOC SPI1_CLK	SOC SPI1_CLK	27
To HSE Connector	SOC SPI1_MOSI	SOC SPI1_MOSI	27
To HSE Connector	SOC SPI1_MISO	SOC SPI1_MISO	27
To HSE Connector	SOC SPI1_CS0	SOC SPI1_CS0	27
To HSE Connector	SOC SPI1_CS1	SOC SPI1_CS1	27
To HSE Connector	SoC I2C0_SCL	SoC I2C0_SCL	15,27,33
To HSE Connector	SoC I2C0_SDA	SoC I2C0_SDA	15,27,33
To HSE Connector	SoC I2C1_SCL	SoC I2C1_SCL	15,19,21,30,31,32,33
To HSE Connector	SoC I2C1_SDA	SoC I2C1_SDA	15,19,21,30,31,32,33
To HSE Connector	CLKOUT0	CLKOUT0	31
To Clock Buffer	SOC MAIN UART0_TX_3V3	SOC MAIN UART0_TX_3V3	26
To Clock Buffer	SOC MAIN UART0_RX_3V3	SOC MAIN UART0_RX_3V3	26
To Clock Buffer	SOC MAIN UART0_CTS_3V3	SOC MAIN UART0_CTS_3V3	26
To Clock Buffer	SOC MAIN UART0_RTS_3V3	SOC MAIN UART0_RTS_3V3	26
To FT4232 Bridge	SOC MAIN UART1_TX_3V3	SOC MAIN UART1_TX_3V3	26
To FT4232 Bridge	SOC MAIN UART1_RX_3V3	SOC MAIN UART1_RX_3V3	26
To FT4232 Bridge	SOC MAIN UART3_RX_3V3	SOC MAIN UART3_RX_3V3	26
To FT4232 Bridge	SOC MAIN UART3_TX_3V3	SOC MAIN UART3_TX_3V3	26

HSE/CAN MUX



CAN INTERFACE



PROC101D(004) TMS84EVM

Project :

Designed for TI by Mistral Solutions Pvt Ltd

Title

CAN & DISPLAY INTERFACE

<Project Name>



Size

Document Number

Rev

C

MS_TI_MAXIE_APPLICATION_CARD_SCH_REVA

D

Date:

Monday, November 27, 2023

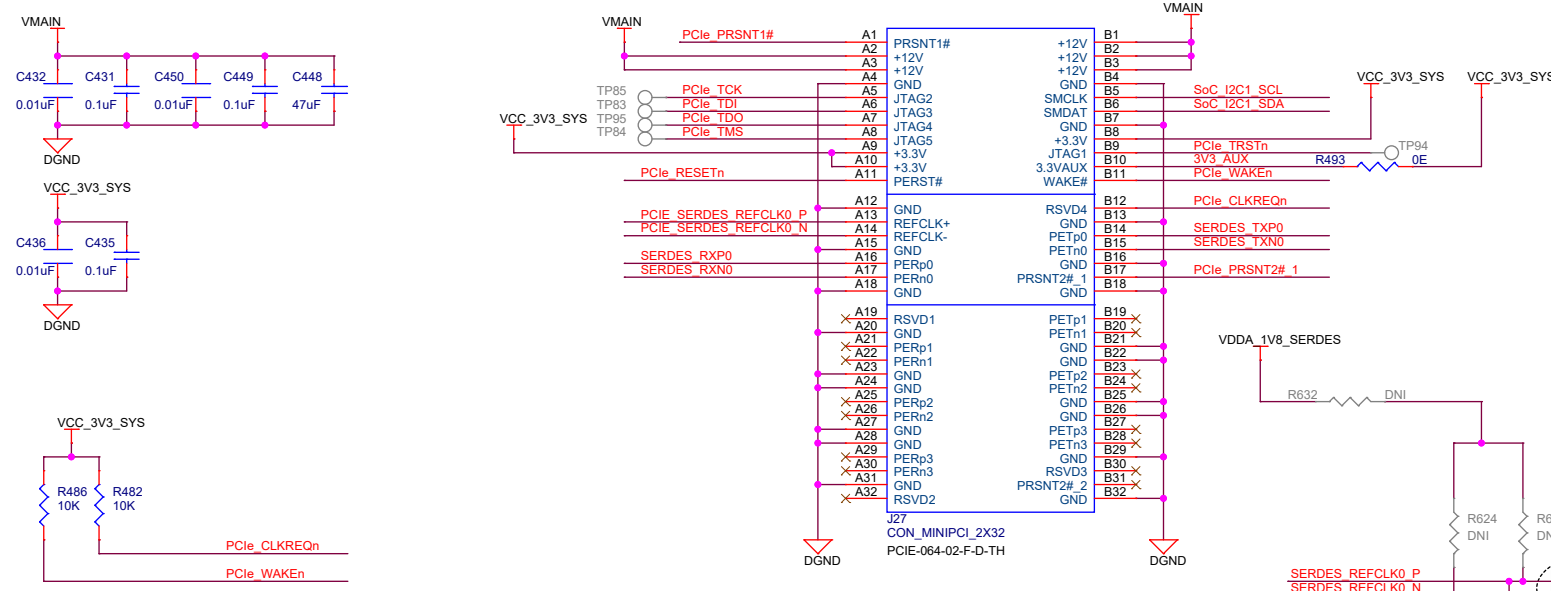
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of

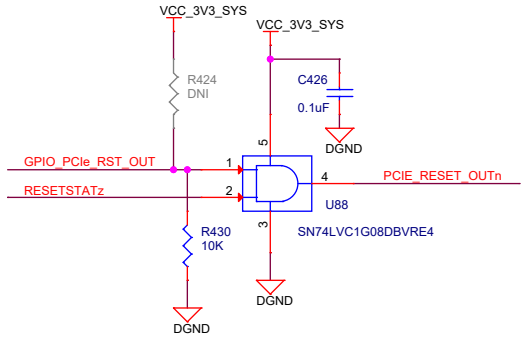
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x4 Lane PCIe Connector

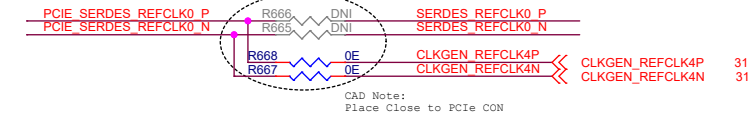


Note:
R679 , R680 Mounted with 0E Resistor when PCIe REFCLK is in no Re-biasing Mode.
R679 , R680 to be replaced with 100nf CAP 0402 package when PCIe REFCLK is in Re-biasing Mode.

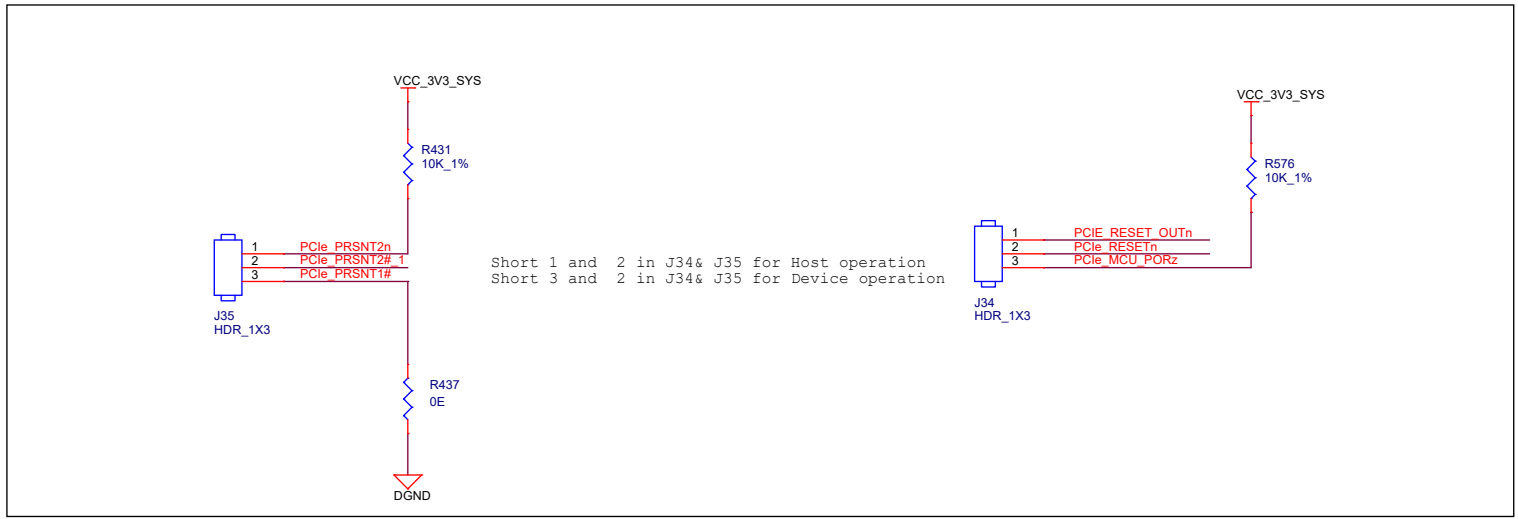
PCIe Reset



CLOCK SELECTION



RC OR EP MODE SELECTION



Off Page Connections

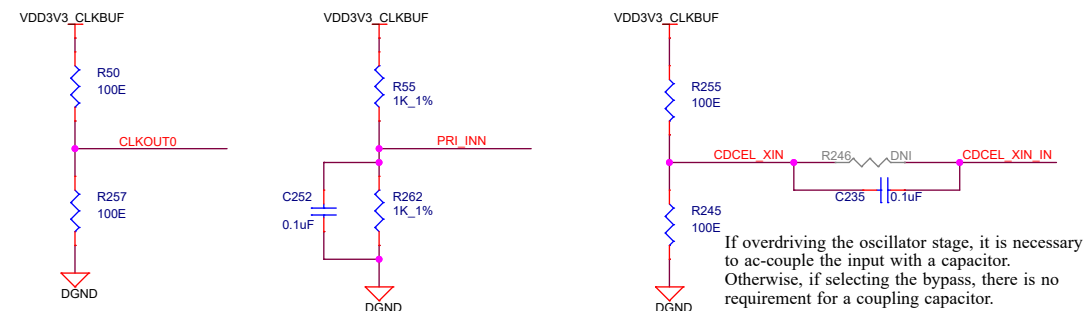
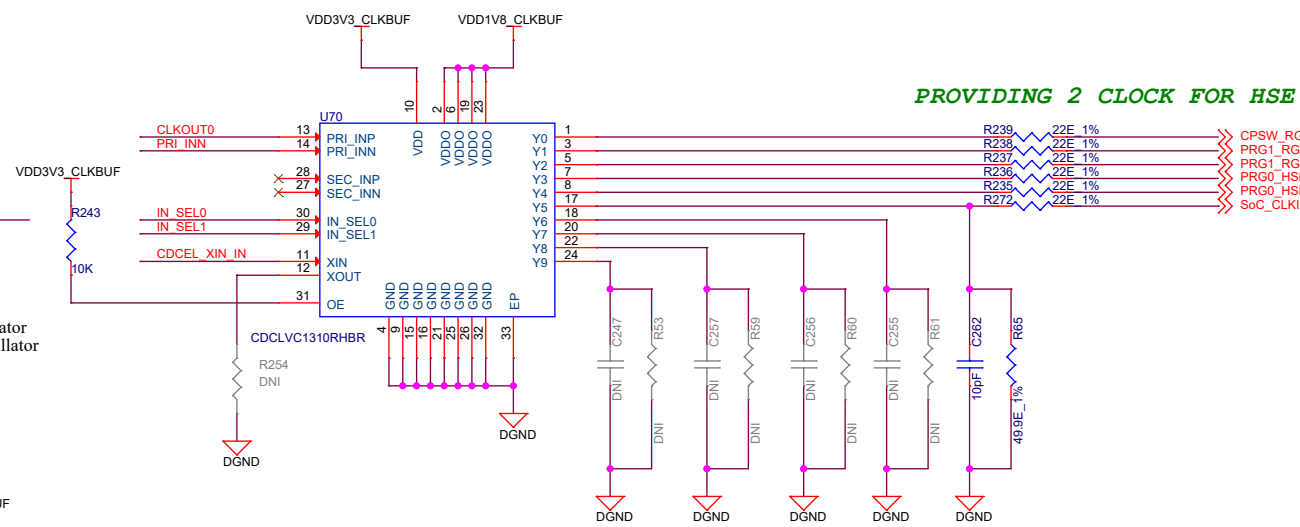
PCIe MCU PORz	PCIe MCU PORz	34
GPIO_PCIE_RST_OUT	GPIO_PCIE_RST_OUT	33
RESETSTATz	RESETSTATz	13,14,20,31,33,34
SoC_I2C1_SCL	SoC_I2C1_SCL	15,19,21,29,31,32,33
SoC_I2C1_SDA	SoC_I2C1_SDA	15,19,21,29,31,32,33

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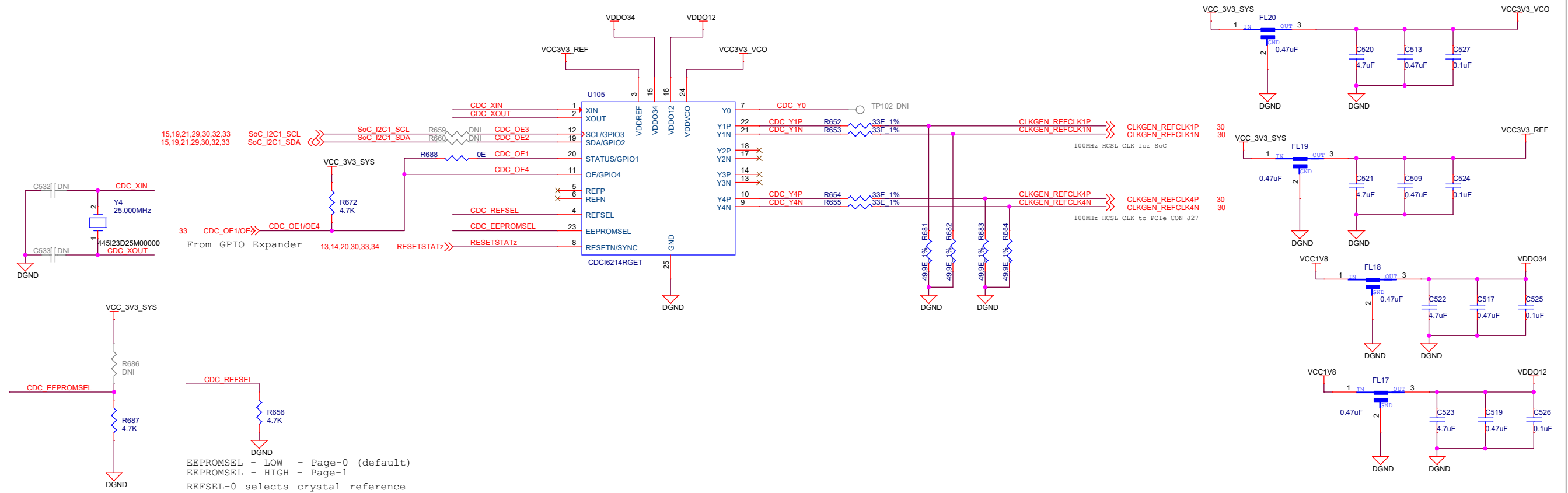


Title PCIe INTERFACE		
Size C	PROC101D(004) TMD84EVM	Rev D
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ETHERNET PHY CLOCK BUFFER



PCIe Clock HCSL (100MHz)



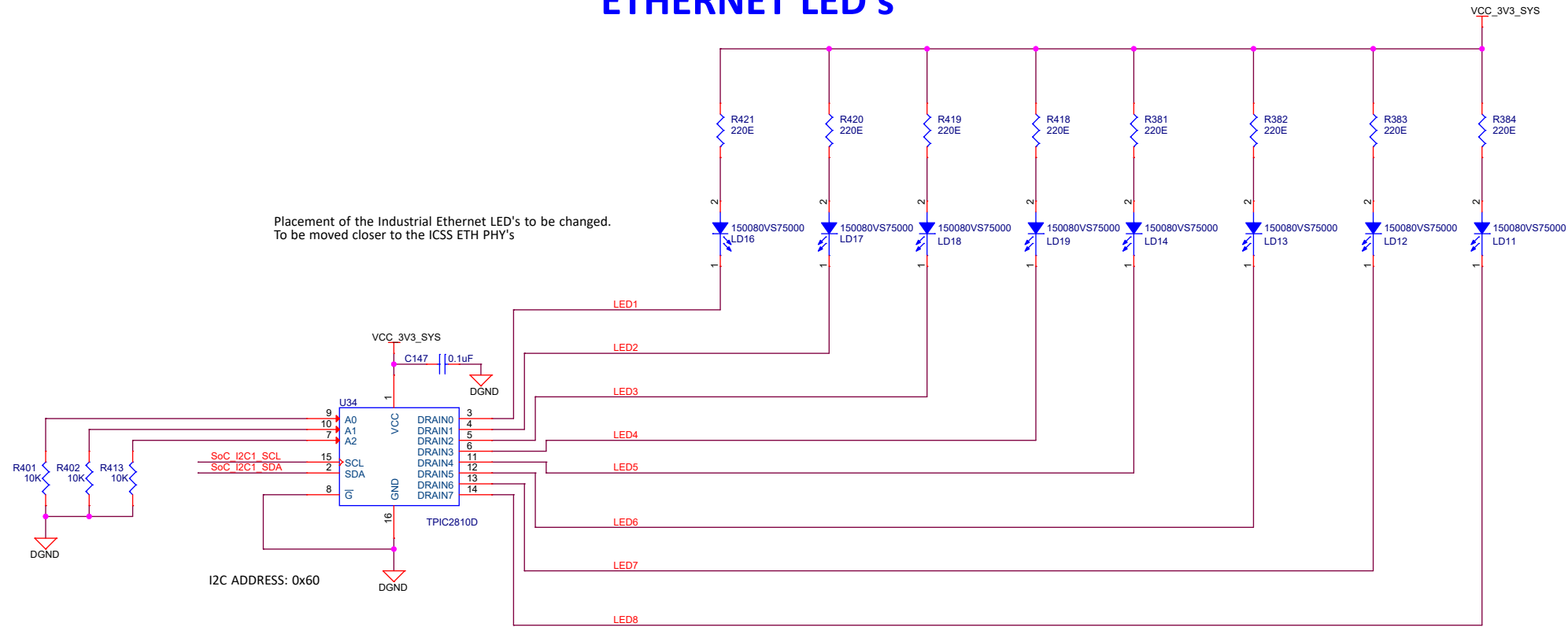
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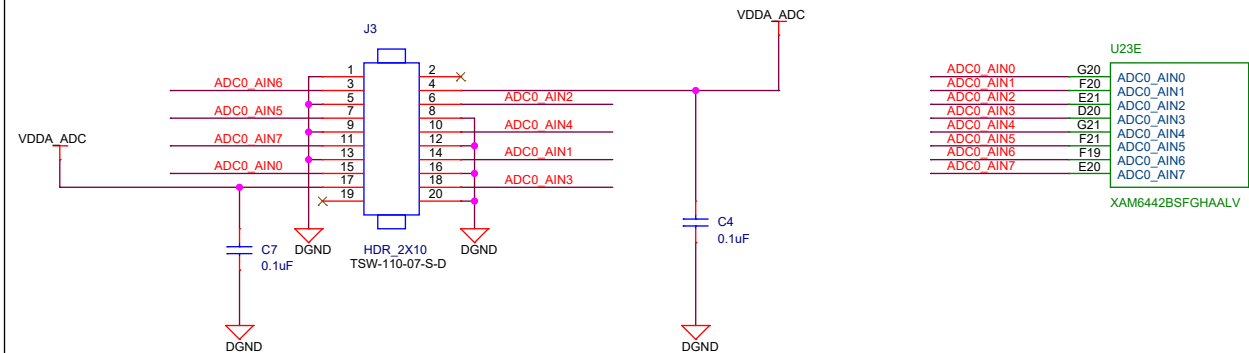
Title	ETHERNET PHY & PCIe CLOCK GENERATOR
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Size	Variant Name = PROC101D(004) TMD564EVM	Rev
C		D
Date:	Monday, November 27, 2023	Sheet 31 of 40

ETHERNET LED's



ADC CONNECTOR



Off Page Connections

SoC I2C1 SCL, SoC I2C1 SDA

SoC I2C1 SCL, SoC I2C1 SDA

15,19,21,29,30,31,33

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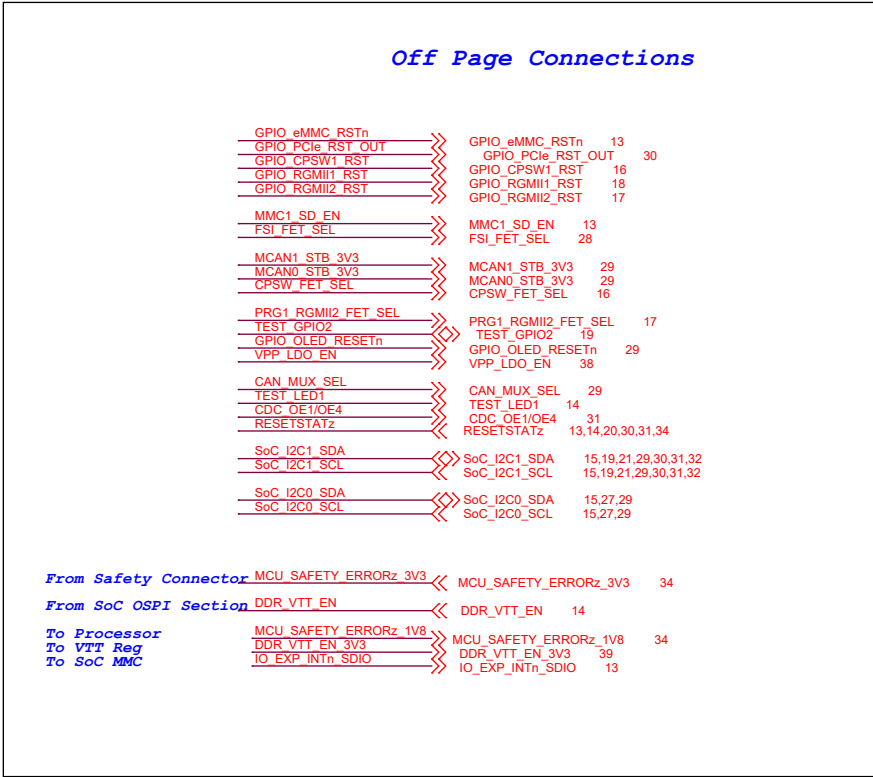
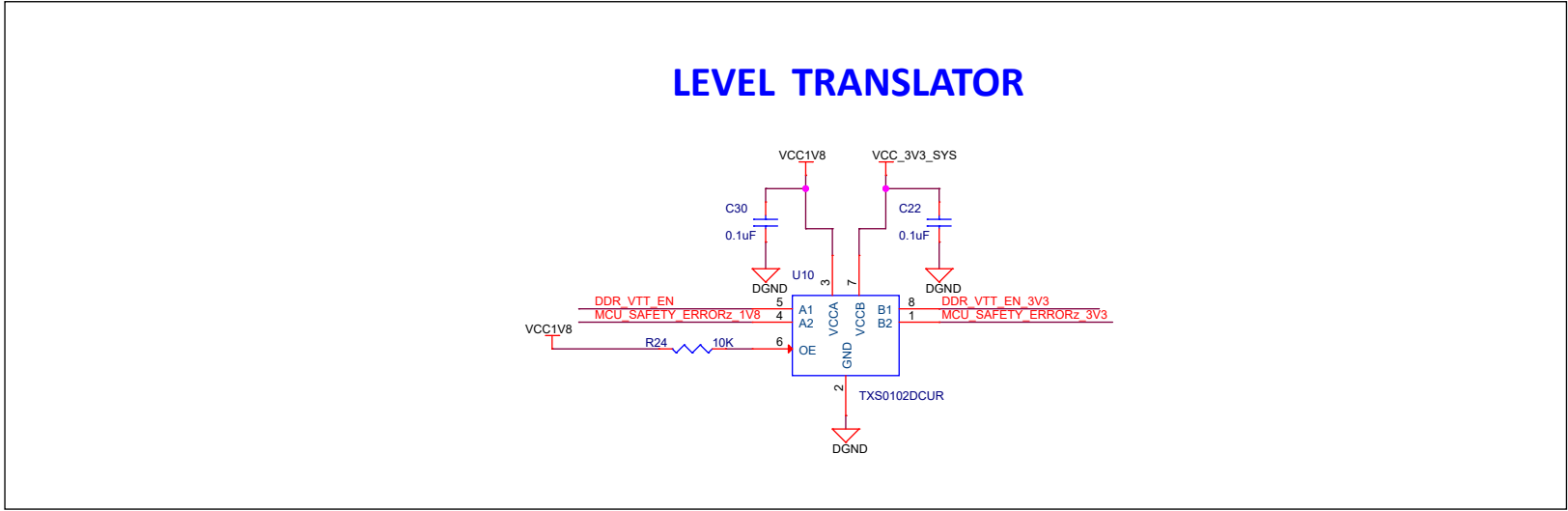
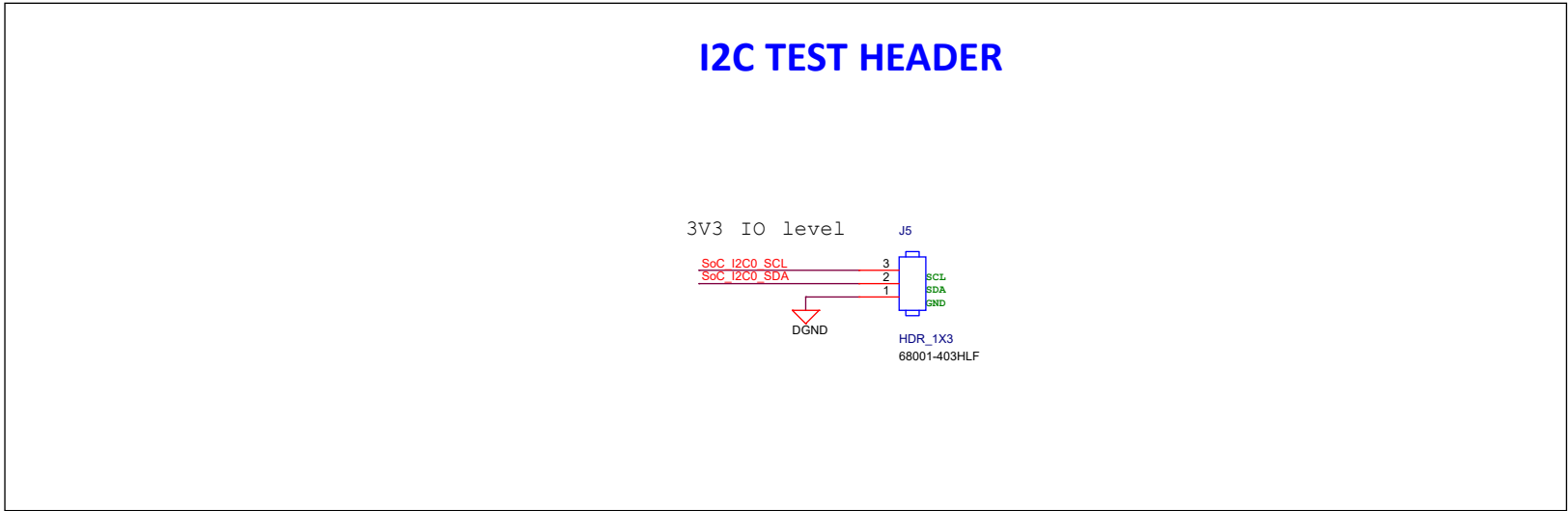
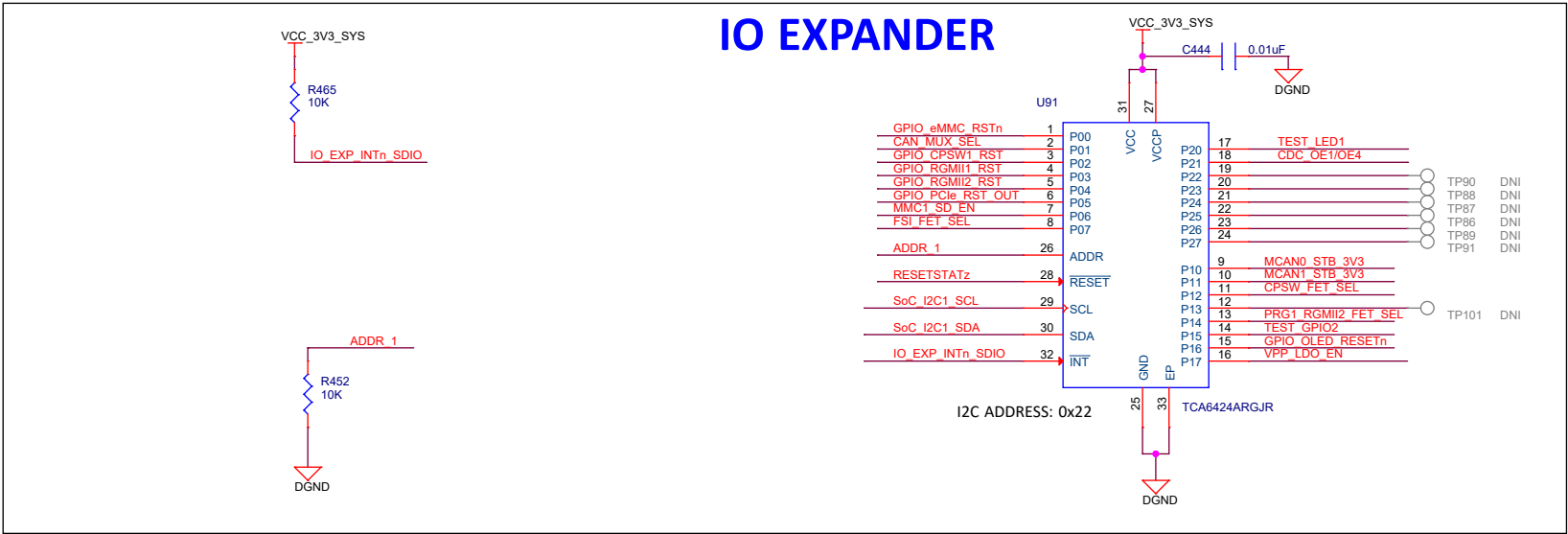
Title ETHERNET LED's

Variant Name = PROC101D(004) TMDS64EVM

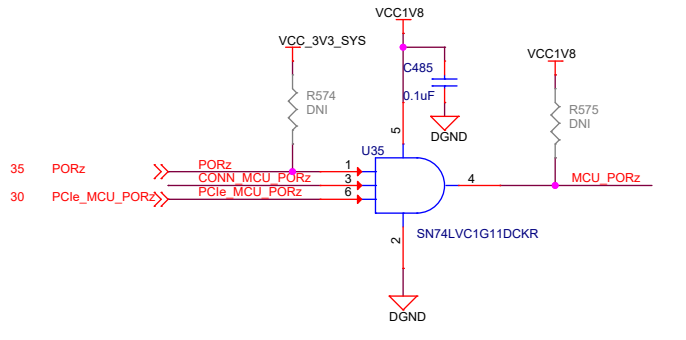
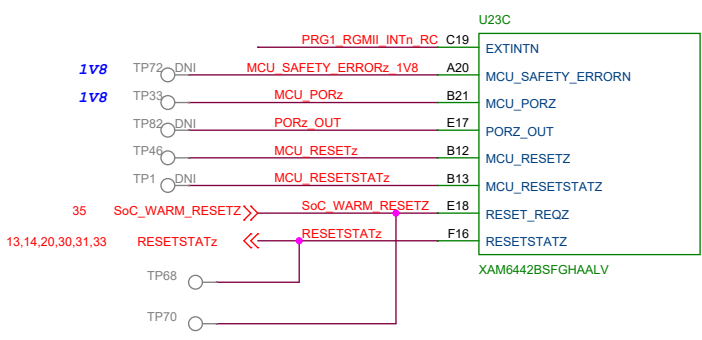
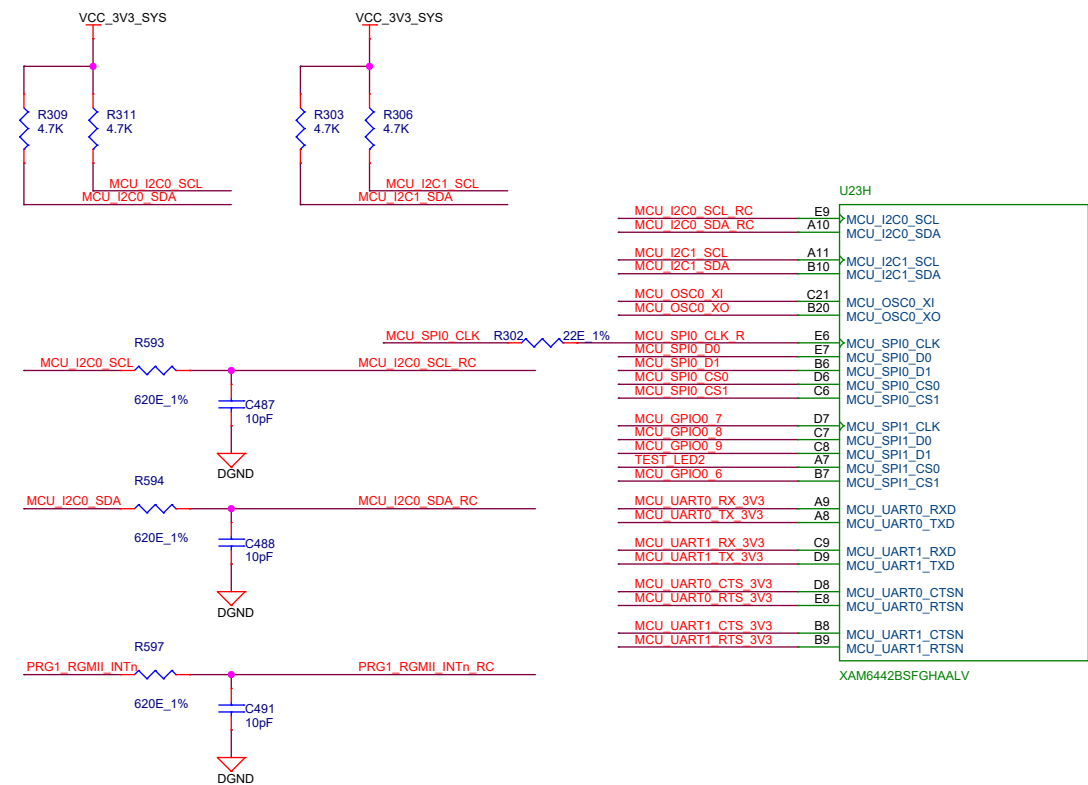
Date: Monday, November 27, 2023

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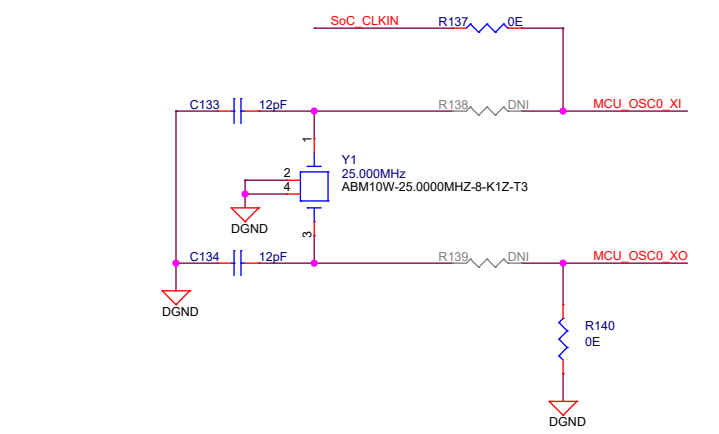
Rev D



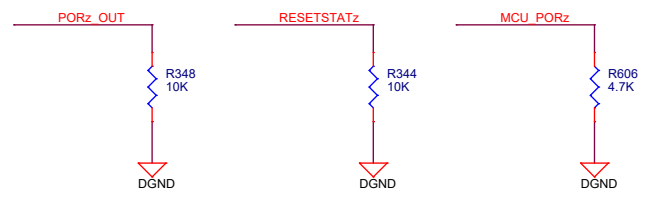
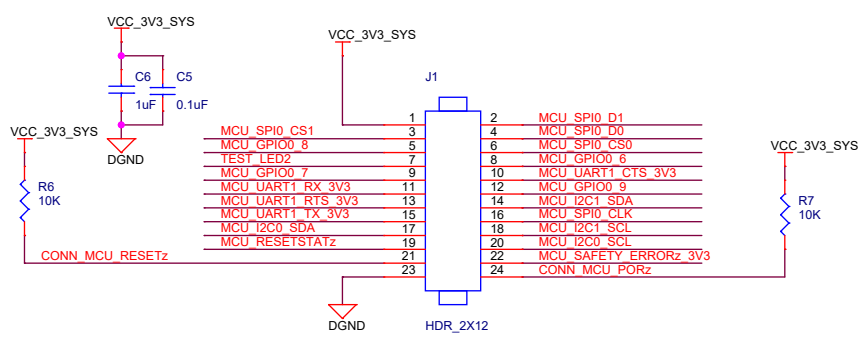
MCU_GENERAL



LPF Designed for 25MHz Cutoff
Have to change resistor and capacitor values accordingly

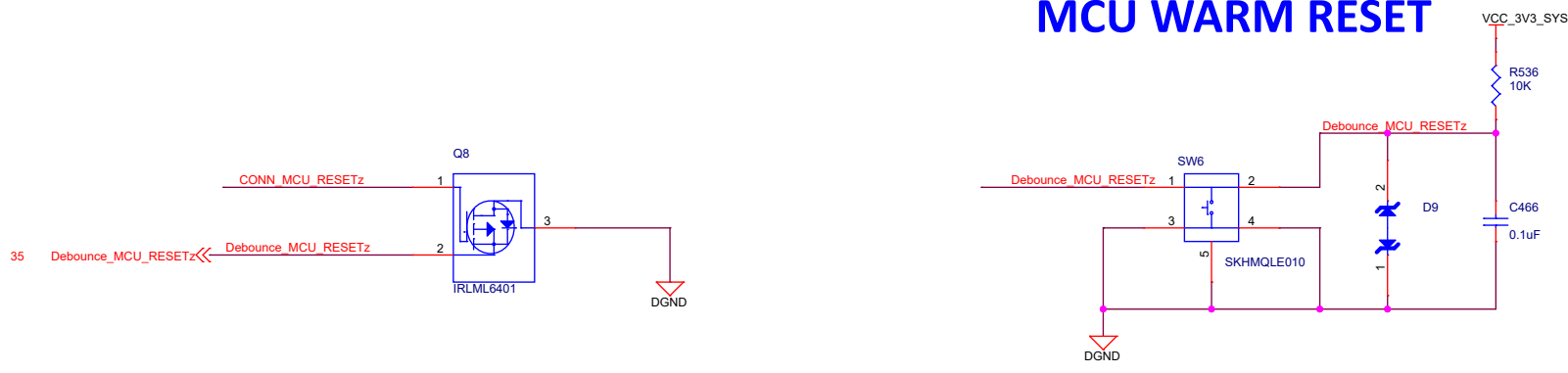


SAFETY CONNECTOR



pull-down resistor on PORz_OUT is provided to keep the signal low until the processor is released from reset during the power-up sequence

MCU WARM RESET



Off Page Connections

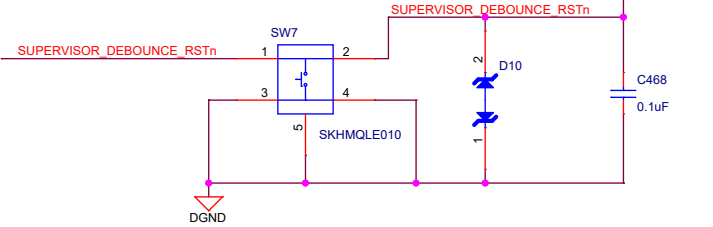
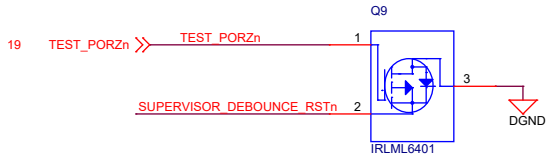
MCU_PORz	MCU_PORz	27
MCU_RESETz	MCU_RESETz	27,35
MCU_RESETSTATz	MCU_RESETSTATz	27
MCU_SAFETY_ERRORz_3V3	MCU_SAFETY_ERRORz_3V3	33
MCU_SAFETY_ERRORz_1V8	MCU_SAFETY_ERRORz_1V8	33
PORz_OUT	PORz_OUT	13,16,17,18,20
PRG1_RGMII_INTn	PRG1_RGMII_INTn	16,17,18
TEST_LED2	TEST_LED2	14
MCU_GPIO0_6	MCU_GPIO0_6	35
SoC_CLKIN	SoC_CLKIN	31
MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	26
MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	26
MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	26
MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	26

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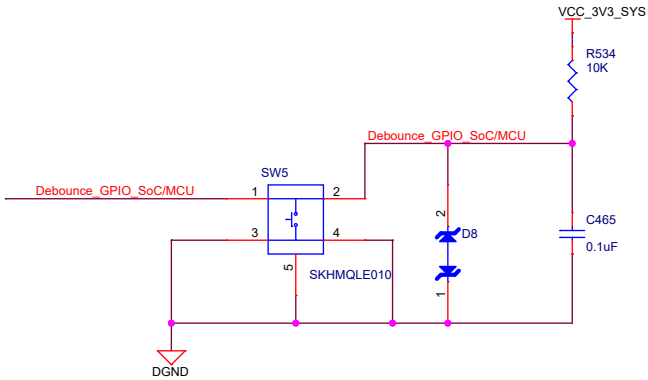
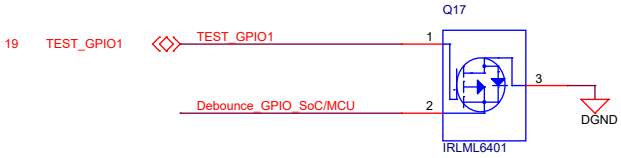
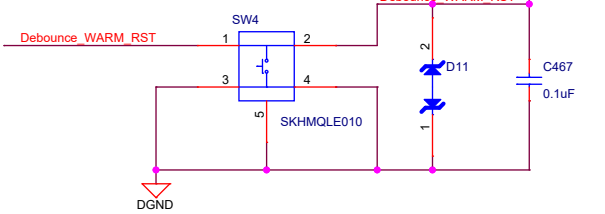
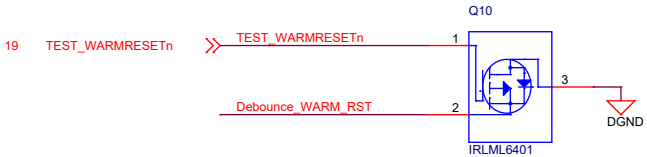


Title MCU GENERAL & SAFETY CONNECTOR		
Size	Variant Name = PROC101D(004) TMDs64EVM	Rev
C		D
Date:	Monday, November 27, 2023	Sheet 34 of 40

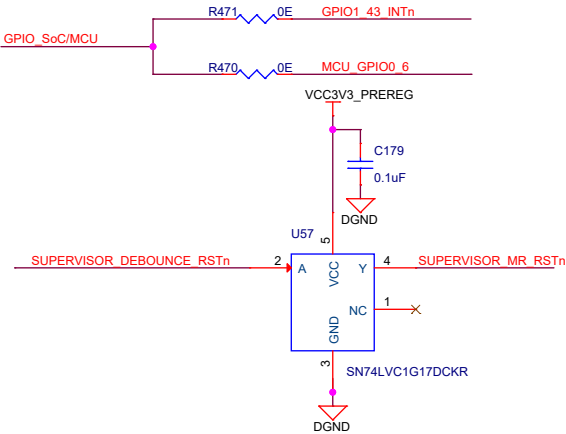
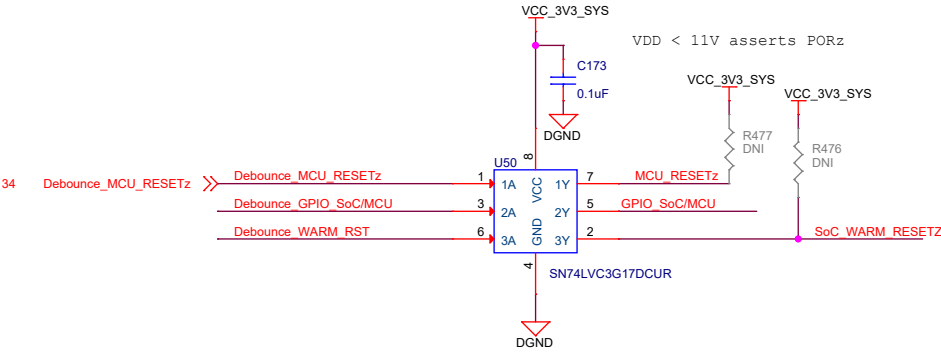
SoC POR_RST



SoC WARM_RST



DEBOUNCE CIRCUIT

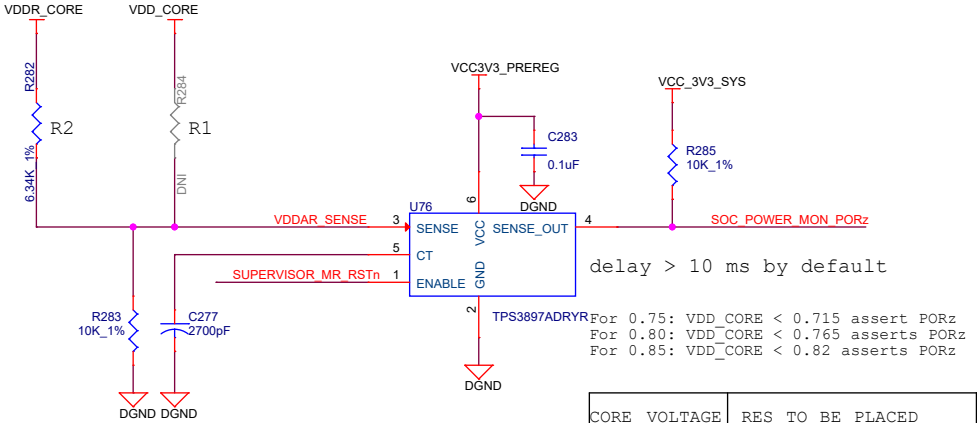


Off Page Connections

To Processor	_VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG	37,39
	_SoC_WARM_RESEZ	SoC_WARM_RESEZ	34
	_GPIO1_43_INTn	GPIO1_43_INTn	29
	_MCU_RESEZ	MCU_RESEZ	27,34
	_MCU_GPIO0_6	MCU_GPIO0_6	34

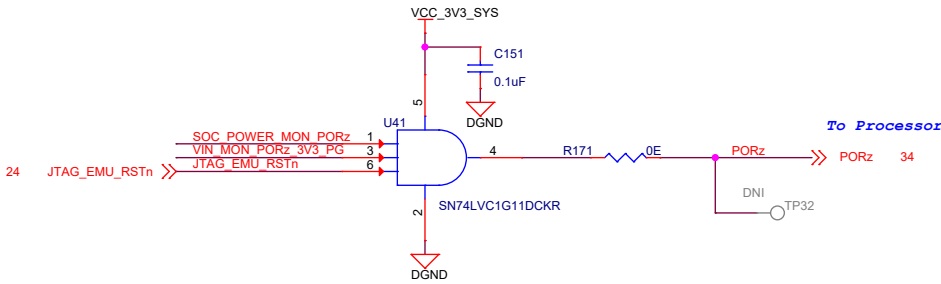
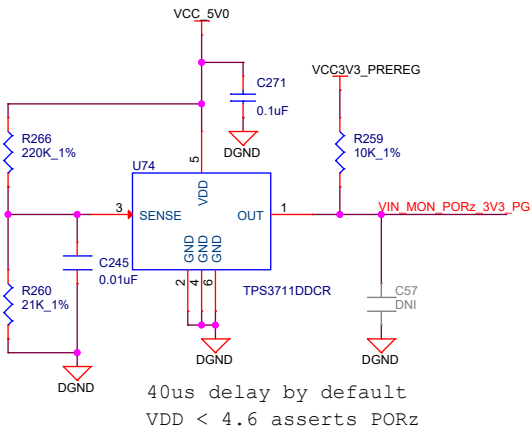
VOLTAGE SUPERVISOR

Core Voltage Monitor (VDDAR_CORE/VDD_CORE)



CORE VOLTAGE	RES TO BE PLACED
0.75V	R1 = 4.3K
0.80V	R2 = 5.23K
0.85V	R2 = 6.34K

5V OUTPUT MONITOR (VCC_5V0)

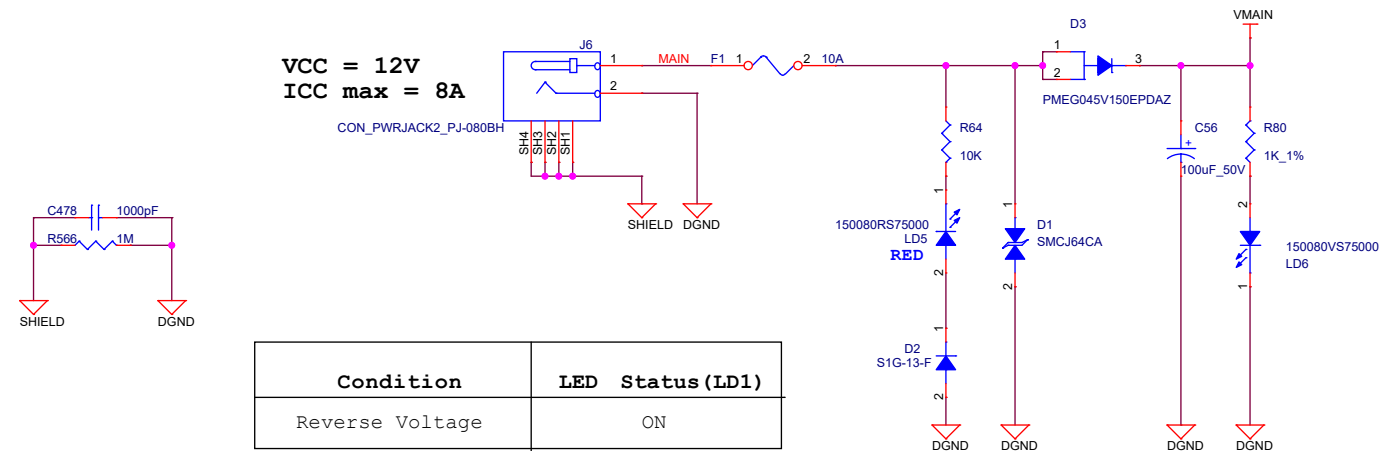


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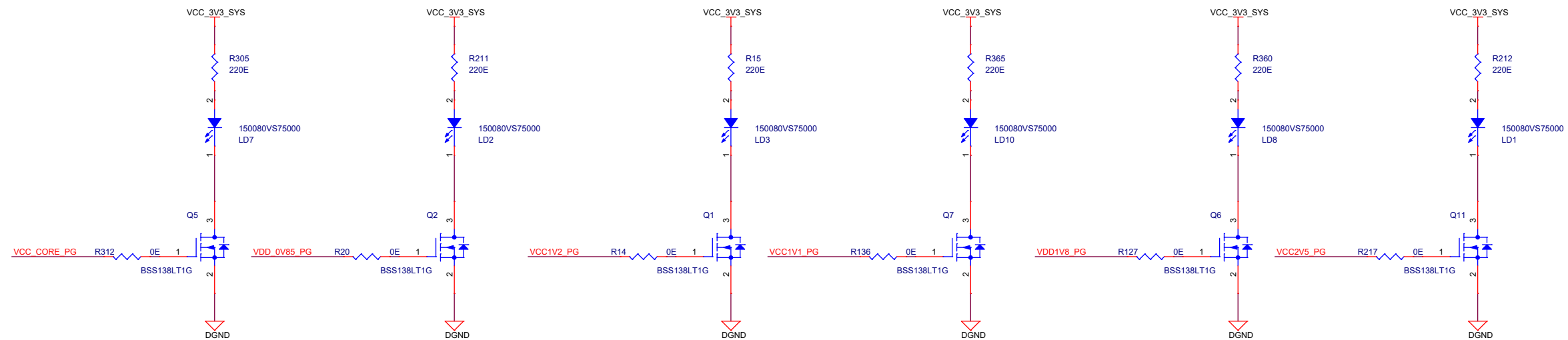


Title			DEBOUNCE CIRCUIT & VOLTAGE SUPERVISOR	
Size			Rev	
C	Variant Name = PROC101D(004) TMDS64EVM		D	
Date:	Monday, November 27, 2023	Sheet	35 of 40	

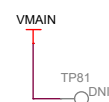
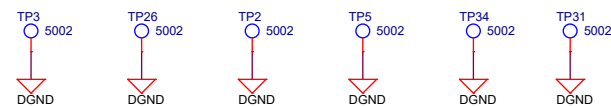
MAIN INPUT 12V DC





POWER INDICATION LED's



Ground test points



Off Page Connections

VCC CORE PG		VCC_CORE_PG	37,38
VDD 0V85 PG		VDD_0V85_PG	38
VCC1V2 PG		VCC1V2_PG	38
VCC1V1 PG		VCC1V1_PG	39
VDD1V8 PG		VDD1V8_PG	38
VCC2V5 PG		VCC2V5_PG	39

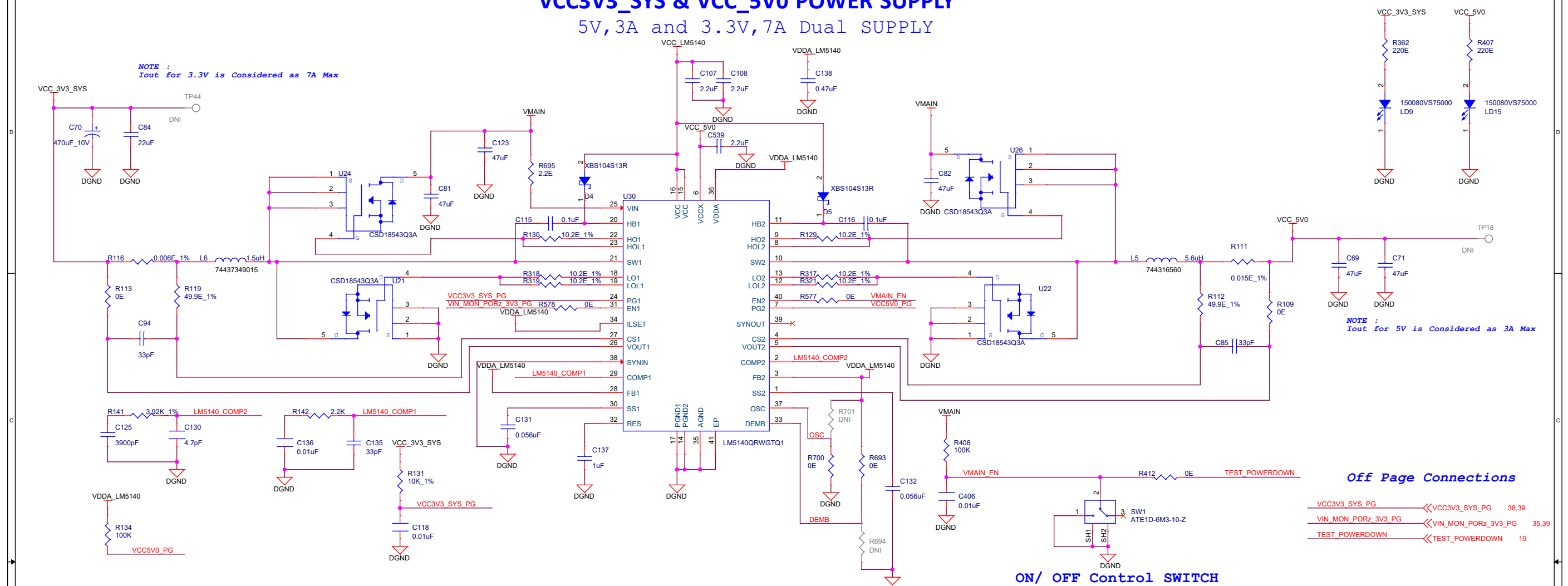
Designed for TI by Mistral Solutions Pvt Ltd



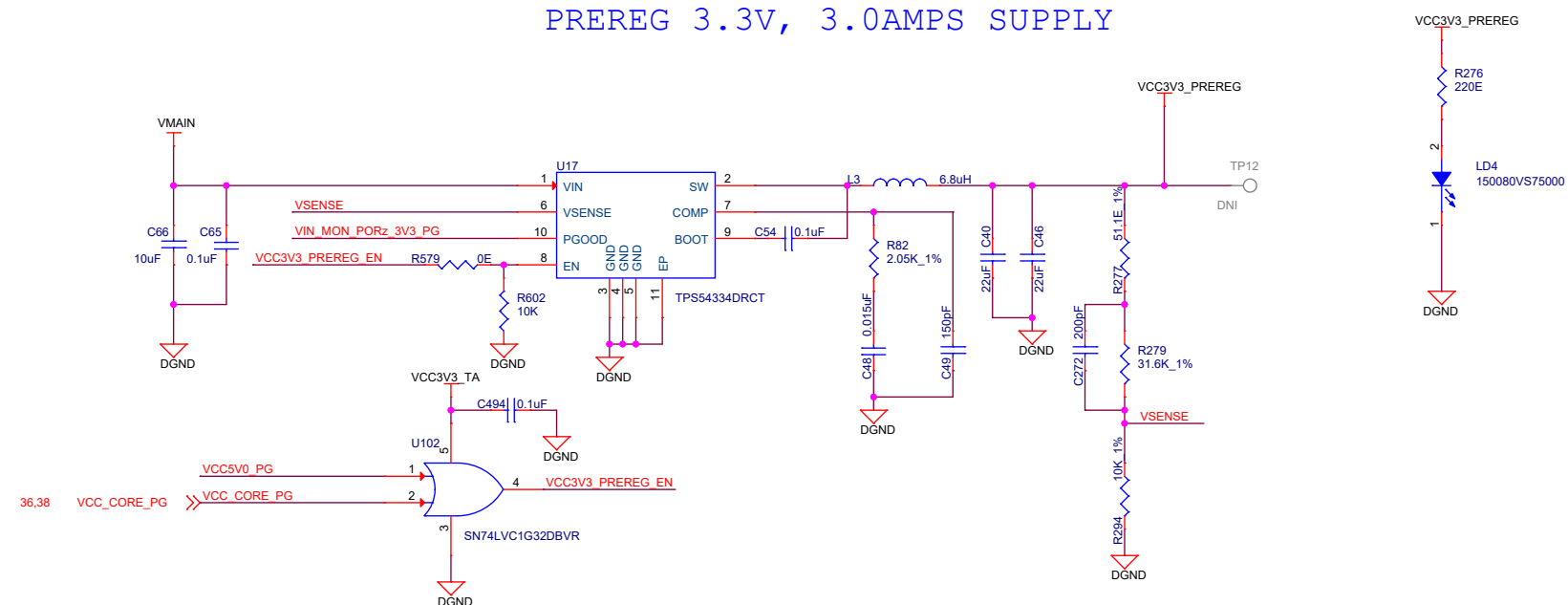
Title	MAIN 12V POWERSUPPLY
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Size	Variant Name = PROC101D(004) TMSD64EVM	R
C		D
Date:	Monday, November 27, 2023	Sheet 36 of 40

VCC3V3_SYS & VCC_5V0 POWER SUPPLY

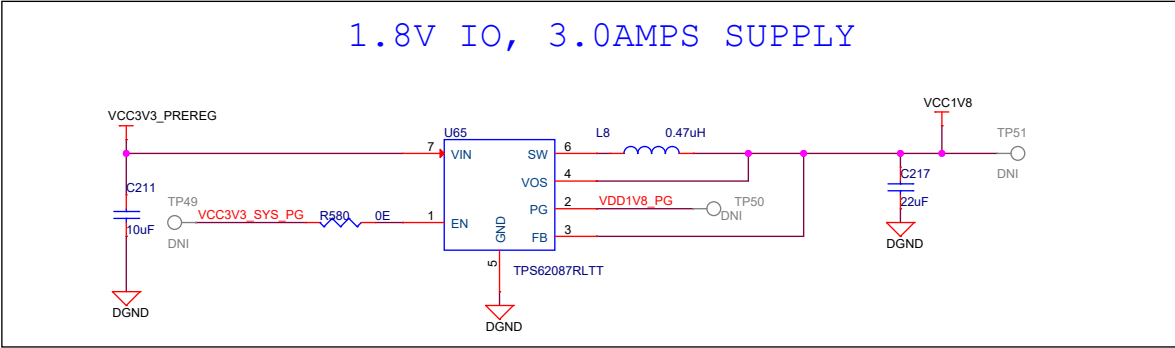


PREREG 3.3V, 3.0AMPS SUPPLY

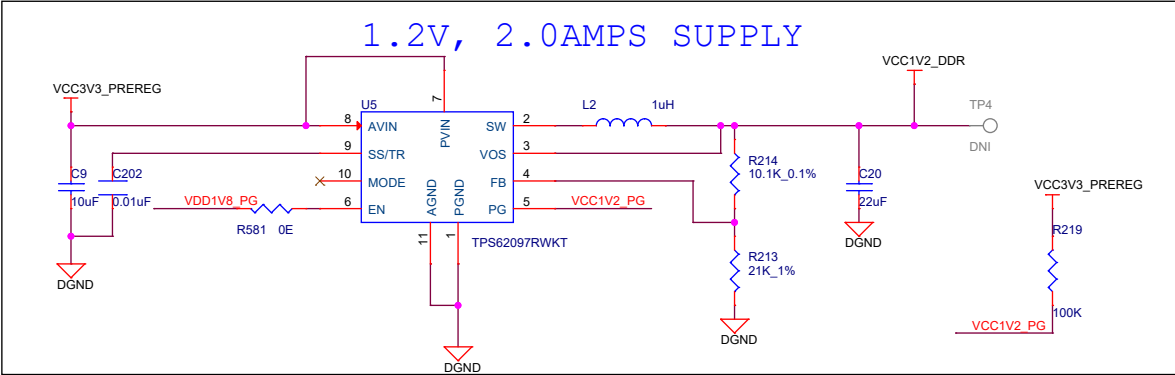


SoC POWER SUPPLY

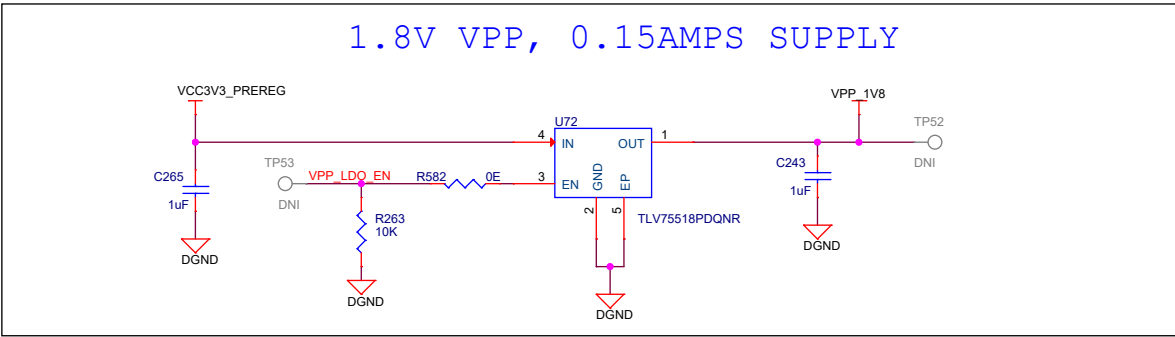
1.8V IO, 3.0AMPS SUPPLY



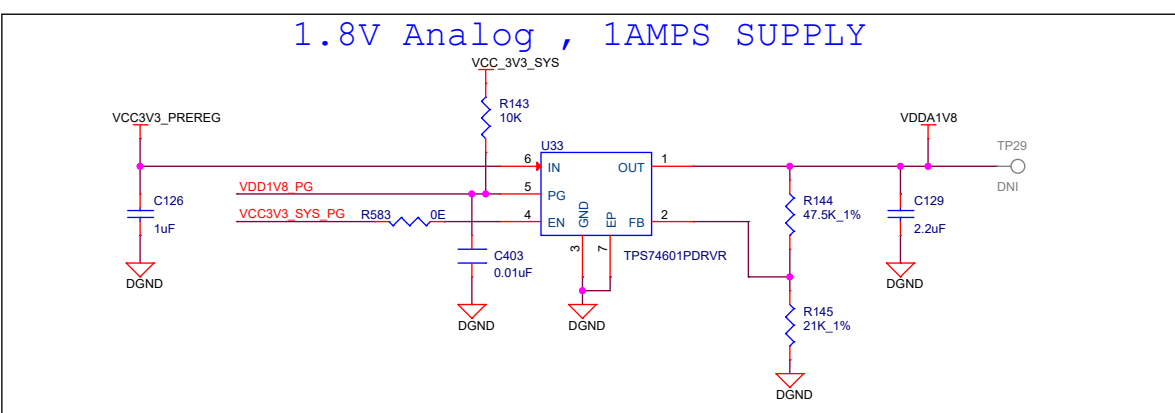
1.2V, 2.0AMPS SUPPLY



1.8V VPP, 0.15AMPS SUPPLY



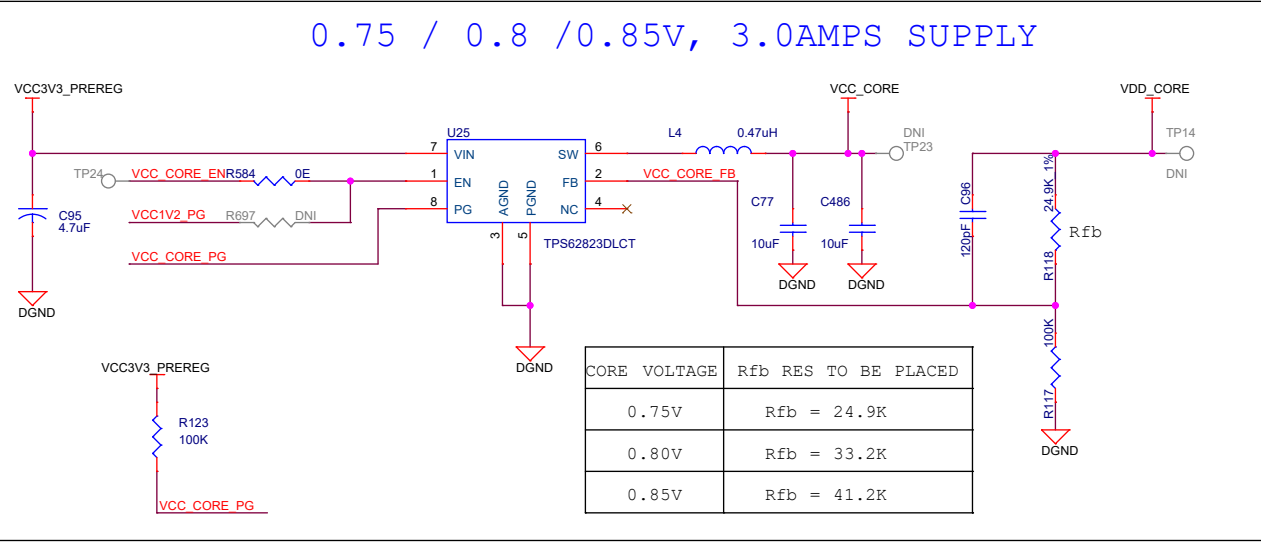
1.8V Analog , 1AMPS SUPPLY



Off Page Connections

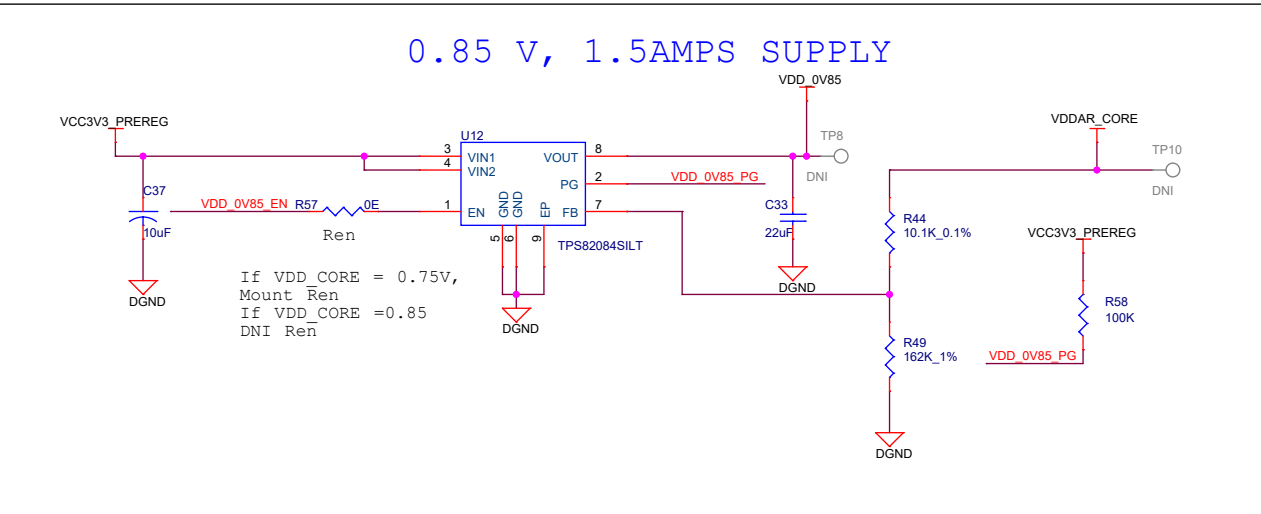
36,37	VCC_CORE_PG	VCC_CORE_PG
36	VDD_0V85_PG	VDD_0V85_PG
36	VCC1V2_PG	VCC1V2_PG
36	VDD1V8_PG	VDD1V8_PG
33	VPP_LDO_EN	VPP_LDO_EN
35,37,39	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG
37,39	VCC3V3_SYS_PG	VCC3V3_SYS_PG

0.75 / 0.8 /0.85V, 3.0AMPS SUPPLY

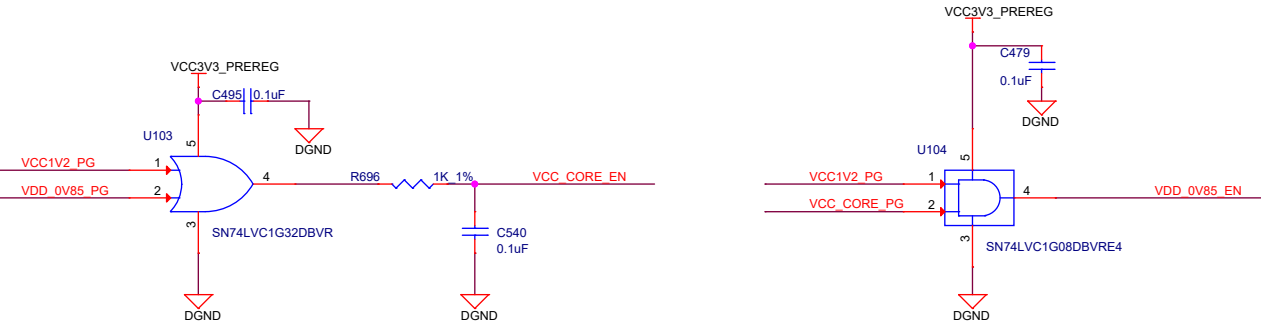


CORE VOLTAGE	Rfb RES TO BE PLACED
0.75V	Rfb = 24.9K
0.80V	Rfb = 33.2K
0.85V	Rfb = 41.2K

0.85 V, 1.5AMPS SUPPLY



If VDD CORE = 0.75V,
Mount Ren
If VDD CORE =0.85
DNI Ren



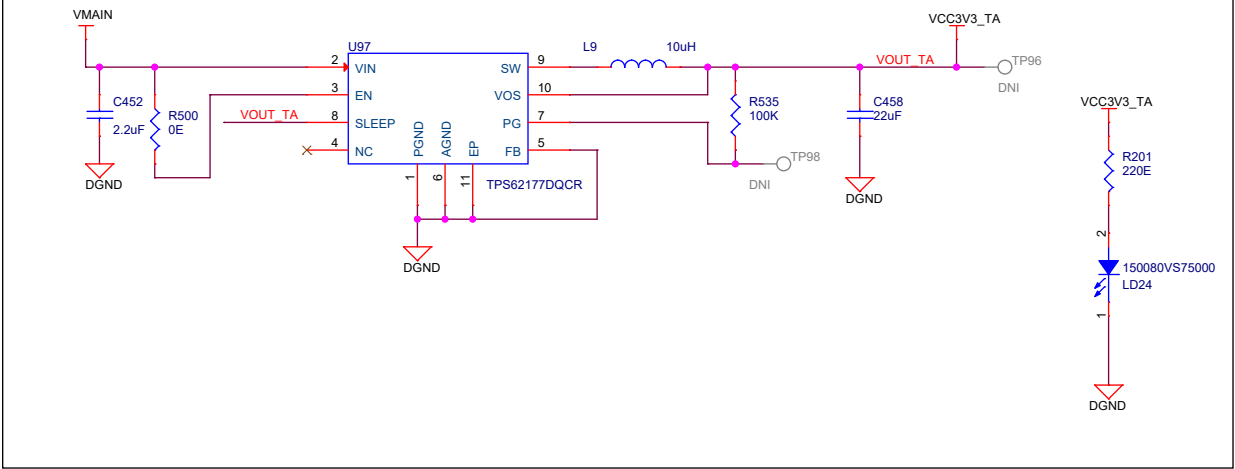
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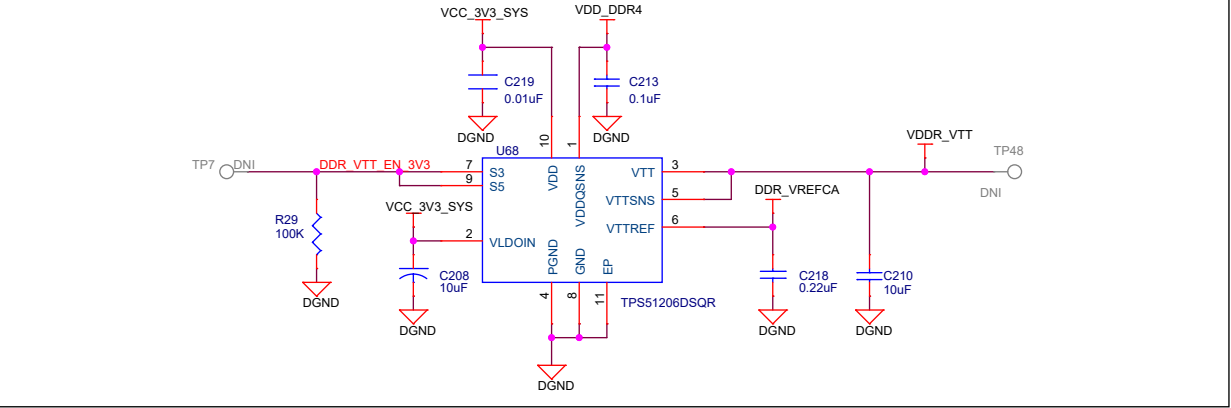
Title SoC POWER SUPPLY		
Size	Variant Name = PROC101D(004) TMDs64EVM	Rev
C		D
Date:	Monday, November 27, 2023	Sheet 38 of 40

PERIPHERAL POWER SUPPLY

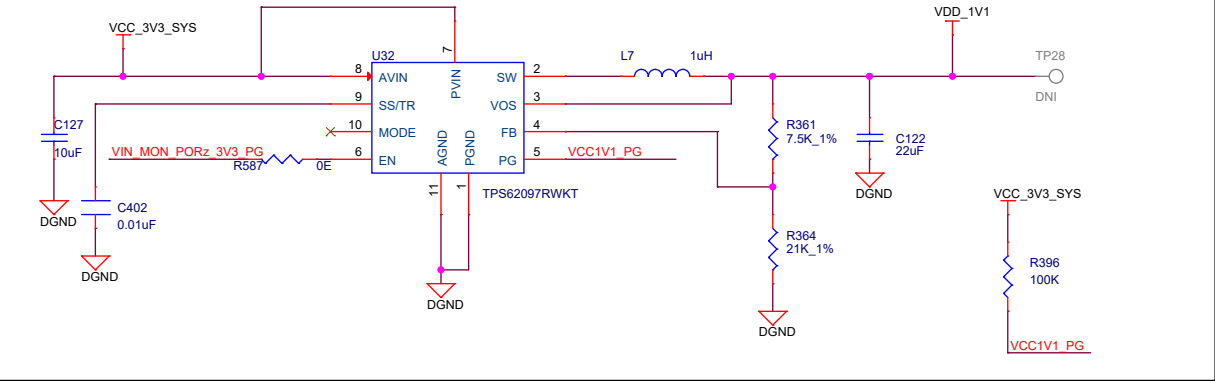
TEST AUTOMATION BOARD POWER



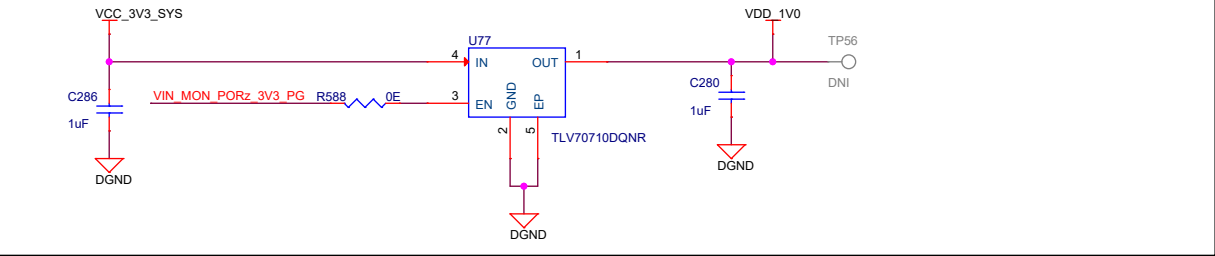
VTT SUPPLY FOR DDR4



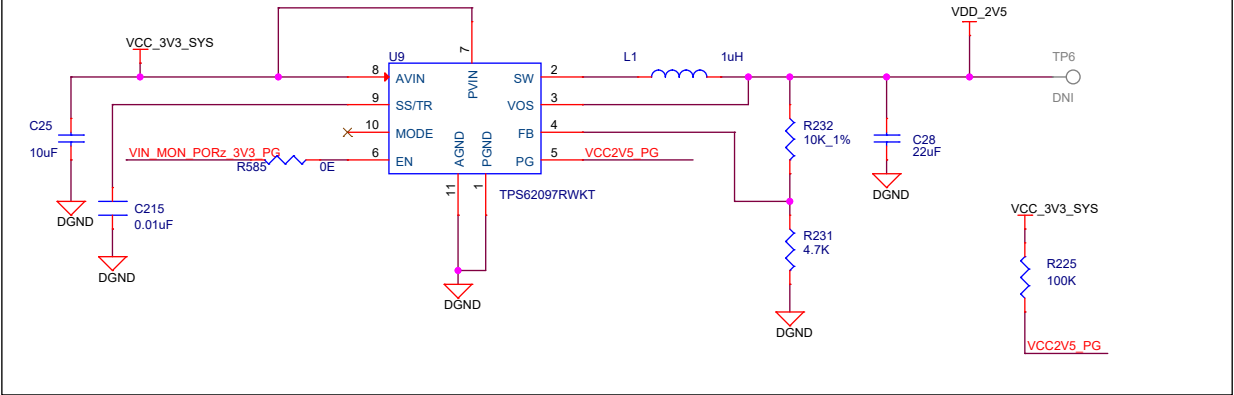
1.1V ETHERNET PHY POWER SUPPLY



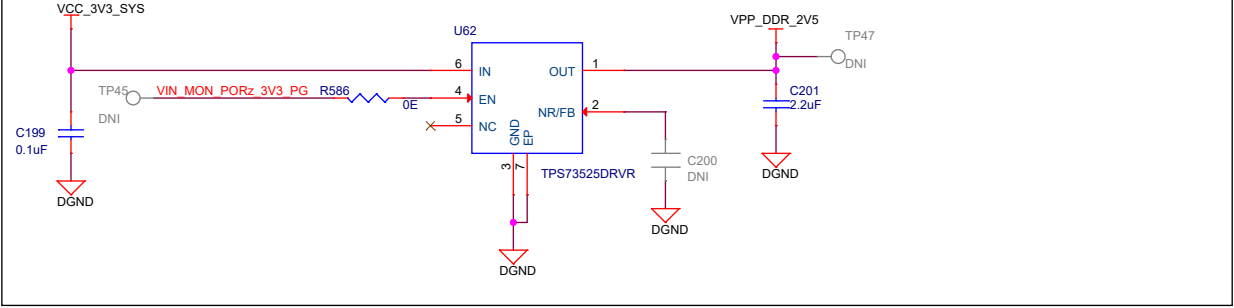
1.0V ETHERNET PHY POWER SUPPLY



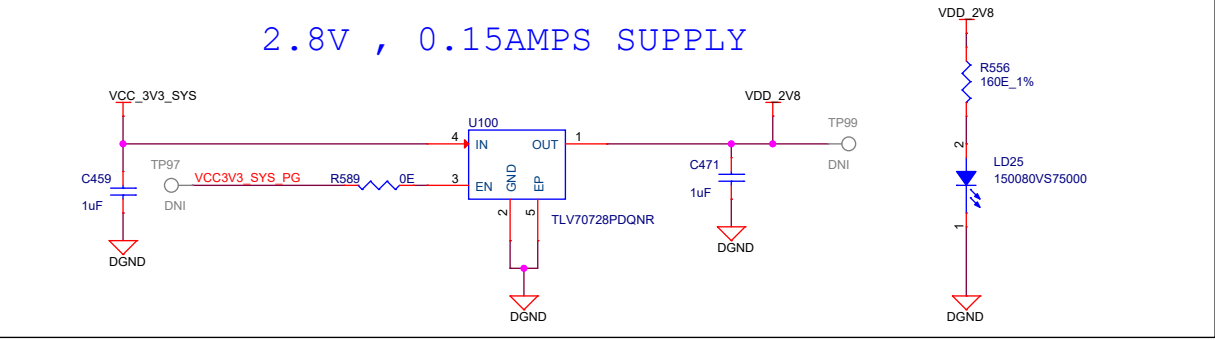
2.5V, 2.0AMPS SUPPLY



2.5V, .5 AMPS SUPPLY



2.8V , 0.15AMPS SUPPLY



Off Page Connections

33	DDR_VTT_EN_3V3	DDR_VTT_EN_3V3
36	VCC2V5_PG	VCC2V5_PG
36	VCC1V1_PG	VCC1V1_PG
37,38	VCC3V3_SYS_PG	VCC3V3_SYS_PG
35,37	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG

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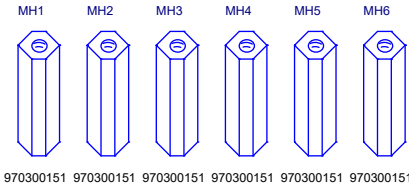
Title PERIPHERAL POWER SUPPLY		
Size	Variant Name = PROC101D(004) TMDs64EVM	Rev
C		D
Date:	Monday, November 27, 2023	Sheet 39 of 40

HARDWARE SCHEMATICS

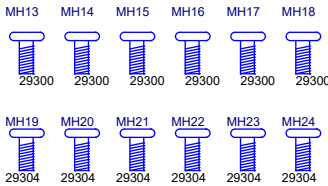
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

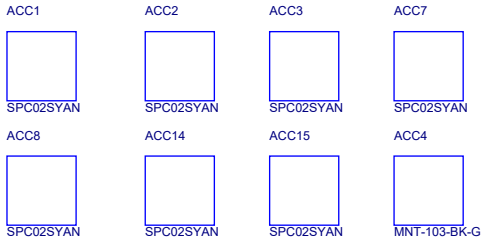
STANDOFFS



SCREWS



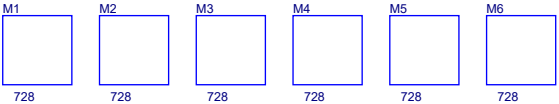
JUMPERS



WASHER's



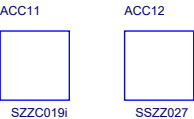
RUBBER FEET



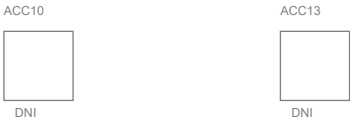
FIDUCIALS



TI EVM FLYERS



Socket & Processor as Accessories



BARE PCB



LABELS

ORDERABLE PART NO

Board Serial No.



Assembly Revision



Orderable part number	
Variant	Label Text
001	TMDS64GPEVM
002	TMDS243GPEVM
003	TMDS64HSEVM
004	TMDS64EVM
005	TMDS243EVM

LOGOs

